SOME INVESTIGATIONS ON UNIFIED POWER QUALITY CONDITIONER

A Thesis Submitted

In Partial Fulfillment of the Requirements

For the Degree of

Doctor of Philosophy

By

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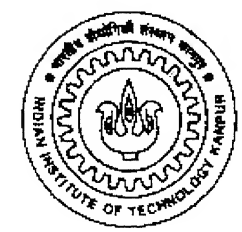

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CERTIFICATE

It is certified that the work contained in this thesis entitled "*Some Investigations on Unified Power Quality Conditioner*", by *Malabika Basu*, has been carried out under our supervision and that this work has not been submitted elsewhere for any degree.

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At the Lotus Feet of

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SYNOPSIS

Power Quality (PQ) has been identified as a major concern for improving system efficiency, minimizing various losses and ensuring production quality. Electric power quality can be broadly classified as a measure of how well electric power is available to customers. When wave shapes deviate from ideal sinusoid, the magnitude of voltage does not pertain to the specified value and the reliability of power supplied is under question, power quality degrades from its desirable standard.

The advent and wide spread use of high power high frequency semiconductor switches over past two decades have given PQ problem a new dimension [1-5]. Because these switches are capable of power conversion with high speed, good control flexibility and high efficiency, they have secured an indispensable position in the processing and utilization of power starting from transmission, distribution to application at very small level. As their non-linear switching actions give rise to consumption of large VAR and current harmonics, non-sinusoidal currents in utility have increased alarmingly, which pollute the supply current and the voltage at the Point of Common Coupling (PCC). Similar to clean environment, clean utility is also the demand of current engineering practices because of several electrical system and equipment hazards like over-heating, increased loss, under utilization of installed capacity, saturation of transformers, mal-triggering of control signal interfaced with utility etc. [4-6].

To protect the interest of utility, international agencies like IEC, IEEE [6] have been developing various standards for harmonic specifications for PCC as well as individual equipment. PQ surveys [1, 2] have been conducted to find out various effects of power

disturbances on industrial production. Voltage sag has been found out to be a major PQ disturbance for which industries suffer huge production losses in terms of material, manpower and money. No specific mandatory standards have come up yet to protect consumer interest from such utility voltage disturbance, though voltage distortion limits have been specified by standards. World wide research on custom power equipment for various Power Quality Control (PQC) measures [7-9] is trying to develop suitable utility interface, which can protect both utility and interest of consumers.

The present dissertation investigates the function of a multi-purpose PQ compensating equipment, ***Unified Power Quality Conditioner*** (UPQC), for non-linear and voltage sensitive loads.

For eliminating harmonic current pollution, shunt Active Power Filters (APF) [10,11] have proved to be the widely accepted solution while to mitigate voltage sag, series injection of voltage with supply is absolutely essential [12, 13]. UPQC being a combination of shunt and series compensators bears advantages of both.

UPQC, unlike Dynamic Voltage Restorer (DVR), does not need any external storage device or additional converter (typically diode bridge rectifier) to supply and maintain the dc link voltage. The common dc link voltage is used by both the series and shunt converters, and shunt converter maintains the dc link voltage through a closed-loop control.

Both single phase [14] and three phase topology [15, 16] of the UPQC have been simulated in SABER and implemented in the laboratory.

The developed UPQC has the following features:

- UPQC eliminates the harmonics in the supply current, thus improves utility current quality for nonlinear loads.
- It provides the VAR requirement of the load, so that the supply voltage and current are always in phase, therefore, no additional power factor correction equipment is necessary. The shunt compensator, which is a Synchronous Link Converter VAR Compensator (SLCVC), is a current controlled VSI that keeps the supply current within a sinusoidal hysteresis band. Therefore, it keeps the THD of supply current low, within the specified standard limit, and the utility has to supply only the fundamental active component of load current.
- UPQC maintains load end voltage at the rated value even in the presence of balanced supply voltage sag.

- The voltage injected by UPQC to maintain the load end voltage at the desired value is taken from the same dc link, thus no additional dc link voltage support is required for the series compensator.
- The injected voltage maintains quadrature advance relationship with the supply current, so no real power is consumed by the series compensator in steady state. This is a big advantage when UPQC mitigates under-voltage conditions. Because of self-sustaining dc bus voltage, duration of sag or under-voltage is not a constraint of operation for UPQC. The series compensator of the UPQC also shares the VAR of the load along with the shunt compensator, so the VA loading of the shunt compensator reduces. To highlight this aspect of quadrature voltage injection, the equipment has been termed as **UPQC-Q** in the dissertation.

A detailed VA loading calculation is performed for a wide range of power factor and sag conditions which brings out the mutual VAR sharing conditions of the two compensators. In the available literature on UPQC, applications for three phase systems are reported. The present dissertation has reported a control scheme suitable for single phase as well as three phase applications. A new PC – based closed-loop hybrid controller has been proposed, combining analog and digital controllers, having good accuracy, speed, flexibility and ease of implementation.

A dynamic sag controller, through a closed loop PI controller, has been proposed which ensures the phase quadrature relationship in case of variable voltage sag and variable load. Detailed design simulations in SABER simulator and experimental implementation on a laboratory prototype have been performed for single phase and three phase UPQC-Q to verify the theory.

Another control scheme for *unbalanced sag mitigation* with the help of UPQC has been designed and simulated in SABER. d-q-o component based synchronously rotating frame analysis has been adopted in this case for dynamic sag controller, with a closed loop control to ensure that voltage injected during sag is appropriate. During balanced voltage sag, the injected voltage is found to be in phase with the supply current, therefore the series compensator is only active power consuming device and acts as a dc load to the dc link capacitor. To highlight this aspect, the system is termed as **UPQC-P** in the thesis. A detailed VA loading analysis has been carried out for different load power factor and sag conditions. Results confirm the effectiveness of the proposed control technique.

The dissertation also envisages a possibility of efficient utilization of parallel converters as VAR compensators and Active Power Filters (APF) for large power loads, by sharing suitable responsibility, which is according to the nature and capacity of the semiconductor switches [17]. Due to limited power handling capacity of individual devices, paralleling is the choice to increase rating of equipment while keeping the THD of the current at PCC within the agency specified standards.

It has been reported in literature that paralleling several converters rather than switches is more reliable in sharing of load largely due to thermal coupling problem. In this perspective, multilevel converters carry lot of weight, as their typical power circuit configuration limits the stress on individual devices to an appreciable extent. Also they bear the advantage of low switching frequency and full utilization of switching devices, which is very essential in high power applications. These favorable advantages have been utilized in parallel combination with a low power high frequency current controlled APF, such that the higher order harmonics can be eliminated. A new parallel converter topology with a three-level Neutral Point Clamped (NPC) converter and an auxiliary current controlled VSI has been proposed and control techniques have been developed. Extensive simulation study has been carried out in SABER simulator for linear and non-linear loads, and performance has been compared with a combination of standard six-step main converter and the auxiliary APF. This study is useful in the design of UPQC for high power application.

The work presented in this thesis is organized as follows.

Chapter 1 introduces the necessity of Power Quality Conditioners from the perspective of different PQ issues and problems.

A review on Power Quality Conditioners has been reported in **Chapter 2**. The three major custom power equipment namely, Shunt (APF), Series (DVR) and Unified compensators (UPQC) are discussed with their different power circuit topology and control philosophy. The detection algorithms for control are discussed. The important observations on Power Quality problems and solutions are summarized.

A single phase UPQC-Q has been proposed in **Chapter 3** with a new closed-loop control strategy. VA loading for different load power factor condition and supply voltage sag has been carried out. Detailed simulation studies have been made. Hardware realizations of the experimental setup followed by experimental results obtained from a laboratory prototype are also presented.

The detailed design, simulation and implementation of UPQC-Q for three phase three wire systems has been reported in **Chapter 4**. The PC based hybrid controller implementation has been described. Simulation and experimental results are presented. In the second part of Chapter 4, a novel control strategy with UPQC-P to mitigate unbalanced supply voltage sag has been proposed. The control theory has been verified through SABER simulation.

A parallel converter scheme suitable for high power load compensation has been reported in **Chapter 5**. A new combination of power circuit topology has been investigated along with suitable control technique. The effectiveness of a three level Neutral Point Clamped (NPC) inverter (high power, low switching frequency, main converter), with a dedicated task of VAR compensation of load at fundamental power frequency is presented. The main converter harmonics and load harmonic currents are compensated by a parallel connected low power high frequency APF. The NPC converter is then replaced by a six-step converter and the performance has been compared.

Chapter 6 summarizes the contributions of the dissertation and gives suggestions for further research in this field.

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δ	Voltage delay angle of the main converter
ω	Angular frequency
α	Firing angle of the converter
ϕ	Power factor angle
θ	Voltage advance angle
$AD_{[i]}$	AD channel of PCL-208, (i stands for channel number)
CH1 CH2	Chopper switch for parallel NPC converter scheme
C_l	Line side filter
con_vd	d –component of supply voltage in SRF frame
con_vo	o –component of supply voltage in SRF frame
con_vq	q –component of supply voltage in SRF frame
D	Anti-parallel diode
DA_0, DA_1	D/A channel of PCL-208
$DAC_{[i]}$	D/A channel of PCL-726, (i stands for channel number)
e_{npc}	NPC converter output voltage
h	Hysteresis window width
i_auxa	Instantaneous auxiliary converter current of phase A
i_load(i)	Instantaneous load currents of phases, (i stands for phase A, B or C)
i_maina	Instantaneous main converter current of phase A
i_{SLCVC}	Instantaneous value of current of shunt compensator (SLCVC)
I_c	Compensator current (rms)
i_c	Instantaneous shunt compensator current
Ic1	Fundamental compensator current
I_{cm1}	Main converter current (fundamental frequency)
$i_{c\alpha}, i_{c\beta}$	Components of the compensator phase currents in α-β coordinates
I_l	Load current (rms)
i_{Lact}	Magnitude of active component of load current
i_{Lreact}	Magnitude of reactive component of load current

$i_{main\ react}$	Magnitude of reactive component of main converter current
$I_{ref(mag)}$	Peak amplitude of reference supply current
i_s	Instantaneous supply current
I_s	Utility current (rms)
i_s^*	Instantaneous reference utility (supply) current
i_{sa}, i_{sb}, i_{sc}	Instantaneous supply (utility) currents of phases A, B, C
I_{sc}	Short circuit current
i_α, i_β	Components of the utility phase currents in α-β coordinates
L_1, L_2	Line inductor
L_a	Inductance associated with auxiliary converter
L_i, C_i	Inverter side filter
L_m	Inductance associated with main converter
Lp, Rp, Ls, Rs	Transformer parameters
L_{SLC}	Inductance (p.u.) of shunt compensator
m_1	Nominal modulating signal
m_2	Modulating signal at the output of PI controller of the dynamic sag controller
m_3	Final modulating signal
MI	Modulation index
P	Active power of load (dc value)
p	Instantaneous active three phase power
$\tilde{p}$	AC quantity of the active power p
p*	Instantaneous active three phase power reference
q	All portions of phase powers that do not contribute to p
$\tilde{q}$	AC quantity of the reactive power q
Q	Reactive power of load
q*	q reference
S	Converter switch
S_{Ain}, $\overline{S}_{Ain}$	Switching signal input
S_{Aout}, $\overline{S}_{Aout}$	Switching signal output
SCR	Short circuit ratio
T_1, T_2	Transformer
v_load(i)	Instantaneous load voltages of phases, (i stands for phase A, B or C)

V_1, V_2	Level of converter voltage in NPC converter
v75	Sinusoidal template 75° advance
v90	Sinusoidal template 90° advance
v_{a1}, v_{a2}, v_{a0}	Positive sequence, negative sequence and zero sequence component of voltage
V_{c1}	Fundamental compensator output voltage
V_{cm1}	Main converter fundamental voltage
v_d, v_q, v_o	Components of the utility phase voltages in d-q-o coordinates
Vdc	DC link voltage
Vdc^*	DC link voltage reference
v_{dref}	d –component of reference supply voltage in SRF frame
$V_{inj(mag)}$	Magnitude of injected voltage of the series compensator
v_{inj}^*	Instantaneous reference injected voltage
V_l	Load voltage (r.m.s)
Vload_ref	Magnitude of reference load voltage
v_{oref}	o –component of reference supply voltage in SRF frame
v_{qref}	q –component of reference supply voltage in SRF frame
V_s	Supply or utility voltage (rms)
Vs_peak	Peak of supply voltage
Vl_peak	Peak of load voltage
v_{sa}, v_{sb}, v_{sc}	Instantaneous source (utility) voltages of phases A, B, C
vsec_[i]	Instantaneous values of injected voltage, i stands for respective phase
v_α, v_β	Components of the utility phase voltages in α-β coordinates
x	p.u. sag
Z_{main}	Impedance associated with main converter
Z_{SLC}	Impedance (p.u.) of shunt compensator

All phasor quantities are represented in bold.

Chapter 1

Introduction

1.1 General Introduction

Power Quality (PQ) Engineering has been a topic of interest from the inception of Power Engineering field. However, with the large growth of non-linear and voltage sensitive loads in the past two decades, Power Quality has become an increased concern for power engineers, and thus it has emerged as an important area of research interest.

Electric Power Quality can be broadly classified as a measure of how well electric power is available to customers. When wave shapes deviate from ideal sinusoid, magnitude of voltage do not pertain to the specified value and reliability is under question, power quality is certainly not at its expected standard, but degraded. The presence of some frequency components, which are attributed as "electrical pollutants", is one of the reasons of poor power quality. Like clean environment, clean utility is also order of the day because of several electrical system and equipment hazards like over-heating, increased loss, under utilization of installed capacity, saturation of transformers, mal-triggering of control signal interfaced with utility etc.

The advent and wide spread use of high power high frequency semiconductor switches have given PQ problem a new dimension. Because these switches are capable of power conversion with high speed, good control flexibility and high efficiency, they have secured an indispensable position in the processing and utilization of power starting from transmission, distribution to application at very small level. As their non-linear switching actions give rise to consumption of large VAR and current harmonics, non-linear currents in utility have increased alarmingly, which pollute the supply current and the voltage at Point of Common Coupling (PCC). This necessitates the use of additional system to maintain quality of desired wave shape and magnitude. Therefore, power quality control has become essential. Further, due to deregulation in the power sectors of transmission and

distribution, Power Quality (PQ) has become a distinguished feature as it is expected to be treated as commodity in the open market economy.

1.2 Importance of PQ Problem

Power Quality problems were brought into concern since the 70's. Industrial consumers and utilities began to apply power factor improvement capacitors to reduce MVA demand from utility grid systems by supplying reactive power demand of the load locally. Further, widespread application of thyristors to drives, converters and voltage regulators brought the effect of harmonics and its associated problems to notice.

Additional methods for dealing with harmonics are necessary for three main reasons:

- The use of static power converters has recently proliferated
- Network resonance have increased
- Power system equipments and loads are more sensitive to harmonics

1.2.1 Importance of understanding harmonics and its effect

The examples of voltage and harmonic sensitive loads and harmonic producing loads are computers, computer controlled machine tools, photo-copying machines, various digital controllers, adjustable speed drives, Programmable Logic Controllers (PLC) etc., which usually have uncontrolled or phase controlled rectifiers on the front-end.

The effects of harmonics are noted below [1-3].

- Harmonics can cause damaging dielectric heating in underground cables
- Inductive metering can be adversely affected by harmonics
- Capacitor bank failures are frequently caused by harmonics
- Additional heating problems in transformers due to increased core losses.
- Interference in communication systems

Therefore, it is observed that presence of harmonics has adverse effect on power systems, consumer load and communication circuits.

The ongoing research has chiefly classified the "Custom Power Solutions" in two categories [14].

a)Local Solution : This calls for the following measures in design of equipments by

- Providing "ride-through" capability to the equipments so that they can be protected against certain amount of voltage sag and swell.
- Equipments that draw non-linear currents are provided with appropriate "front-end" correcting devices and control, which can do active wave shaping, so that they do not draw currents of undesirable nature from the utility.

But the criticism against these types of solution is that it cannot provide solution to already existing electrically polluting installations. Replacement and redesign also do not sound techno-economical. Secondly, if for every small equipment, front-end wave shaping is incorporated, the cost will be significantly more, which may not be a viable solution for customers.

b)Global Solution: Considering the practical limitation and the techno-economical issues involved in the above approach, system solutions, which are more general in nature, are envisaged.

- Here independent compensating devices are installed at PCC or other selected locations, so that overall power quality improves at the PCC.
- Individual equipments need not be designed according to PQ standards.
- Already existing pollutants can be well taken care of.

Since early 80's with the applications of modern self-commutating switching devices, VSI and CSI's have been put to use as Active Power Filters (APF) and Synchronous link Converter VAR Compensators (SLCVC) to compensate for load VAR, current harmonics, and Dynamic Voltage Restorer (DVR) for voltage support. Due to very fast and good controllability of these switches, high control bandwidth has been attained. Additionally, due to availability of fast acting controllers like PC, DSP, etc., high speed control has been achieved, and real time control applications have been realized.

Efforts are made to minimize the cost of these equipments, by minimizing equipment rating, maximizing their functional capability and making them multi-purpose.

1.5 Scope and Objectives of the Thesis

The present dissertation investigates the function of a multi-purpose PQ compensating equipment ***Unified Power Quality Conditioner*** (UPQC) for non-linear and voltage sensitive loads.

For eliminating current pollution, shunt APFs have proved to be the widely accepted solution while to combat voltage sag, series injection of voltage with supply is absolutely essential. UPQC being a combination of shunt and series compensators bears advantages of both.

UPQC, unlike Dynamic Voltage Restorer (DVR), does not need any external storage device or additional converter (typically diode bridge rectifier) to supply and maintain the dc link voltage. The common dc link voltage is being used by both the series and shunt converters, and the shunt converter maintains the dc link voltage through a closed-loop control.

Both single phase and three phase topology of the UPQC have been simulated in SABER and implemented in the laboratory.

The developed UPQC has the following features:

- UPQC eliminates the harmonics in the supply current, thus improves utility current quality for nonlinear loads.
- It provides the VAR requirement of the load, so that the supply voltage and current are always in phase, therefore, no additional power factor correction equipment is necessary. The shunt compensator, which is a Synchronous Link Converter VAR Compensator (SLCVC), is a current controlled VSI that keeps the supply current within a sinusoidal hysteresis band. Therefore, it keeps the THD of supply current low, within the specified standard limit, and the utility has to supply only the fundamental active component of load current.
- UPQC maintains load end voltage at the rated value even in the presence of balanced supply voltage sag.
- The voltage injected by UPQC to maintain the load end voltage at the desired value is taken from the same dc link, thus no additional dc link voltage support is required for the series compensator.
- The injected voltage maintains quadrature advance relationship with the supply current, so no real power is consumed by the series compensator in steady state. This is

a big advantage when UPQC mitigates under voltage conditions. The series compensator of the UPQC also shares the VAR of the load along with the shunt compensator, so the VA loading of the shunt compensator reduces. To highlight this aspect of quadrature voltage injection the equipment has been termed as **UPQC-Q** in the dissertation.

A detailed VA loading calculation is performed for a wide range of power factor and sag conditions, which brings out the mutual VAR sharing conditions of the two compensators. In the available literature on UPQC, applications for three phase systems are reported. The present dissertation has reported a control scheme suitable for single phase as well as three phase applications. A new PC–based closed-loop hybrid controller has been proposed, combining analog and digital controllers, having good accuracy, speed, flexibility and ease of implementation.

A dynamic sag controller, through a closed-loop PI controller has been proposed which ensures the phase quadrature relationship in case of variable voltage sag and variable load. Detailed design simulations in SABER simulator and experimental implementation on a laboratory prototype have been performed for single phase and three phase UPQC-Q to verify the theory.

Another control scheme for *unbalanced sag mitigation* with the help of UPQC has been designed and simulated in SABER. d-q-o component based synchronously rotating frame analysis has been adopted in this case for dynamic sag controller, with a closed-loop control to ensure that voltage injected during sag is appropriate. During balanced voltage sag, the injected voltage is found to be in phase with the supply current. Therefore, the series compensator behaves as an active power consuming device only and acts as a dc load to the dc link capacitor. To highlight this aspect, the system is termed as **UPQC-P** in the thesis. A detailed VA loading analysis has been carried out for different load power factor and sag conditions. Results confirm the effectiveness of the proposed control technique.

The dissertation also envisages a possibility of efficient utilization of parallel converters as VAR compensators and Active Power Filters (APF) for large power loads, by sharing suitable responsibility, which is according to the nature and capacity of the semiconductor switches. Due to limited power handling capacity of individual devices, paralleling is the choice to increase rating of equipment while keeping the THD of the current at PCC within the agency specified standards.

It has been reported in literature that paralleling several converters rather than switches is more reliable in sharing of load largely due to thermal coupling problem. In this perspective, multilevel converter carries lot of weight as their typical power circuit configuration limits the stress on individual devices to an appreciable extent. Also, they bear the advantage of low switching and full utilization of switching devices, which is very essential in high power applications, and minimization of simultaneous turn-off and turn-on of switches. These favorable advantages have been utilized in parallel combination with a low power high frequency current controlled APF, such that the higher order harmonics can be eliminated. A new parallel converter topology with a three-level Neutral Point Clamped (NPC) converter and an auxiliary current controlled VSI has been proposed and control techniques have been developed. Extensive simulation study has been carried out in SABER simulator for linear and non-linear loads, and performance has been compared with a combination of standard six-step main converter and the auxiliary APF.

This study is useful in the design of UPQC for high power application. While the present topology aims at the compensation of load VAR and harmonics by a shunt connected system, the supply voltage sag can be compensated by an independent series converter with a self sustained dc link. The injected voltage will remain in quadrature advance with the supply voltage such that, the series compensator would not consume active power, except to sustain the dc link voltage for the converter losses. Thus, the voltage sag compensator can be mutually independent of the harmonic and reactive current compensator. The topology and control for this shunt controller scheme being new, the dissertation has also addressed the issues involved in details.

1.6 Organization of the Thesis

The work presented in this thesis is organized as follows

A review on Power Quality Conditioners has been reported in **Chapter 2**. The three major custom power equipments Shunt (SLCVC, APF), Series (DVR) and Unified compensators (UPQC) are discussed with their different power circuit topology and control philosophy. The detection algorithms for control are discussed. The important observations on Power Quality problems and solutions are summarized.

A single phase UPQC-Q has been proposed in **Chapter 3** with a new closed-loop control strategy. VA loading for different load power factor condition and supply voltage sag has been carried out. Detailed simulation studies have been made. Hardware realizations of the experimental setup followed by experimental results obtained from a laboratory prototype are also presented.

The detailed design, simulation and implementation of UPQC-Q for three phase three wire systems has been reported in **Chapter 4**. The PC-based hybrid controller implementation has been described. Simulation and experimental results are presented. In the second part of Chapter 4, a novel control strategy with UPQC-P to mitigate unbalanced supply voltage sag has been proposed. The control theory has been verified through SABER simulation.

Parallel converter schemes suitable for high power load compensation have been reported in **Chapter 5**. A new combination of power circuit topology has been investigated along with suitable control technique. Attempts have been focused on the effectiveness of a three level Neutral Point Clamped (NPC) inverter which can be rated for high power (main converter), as one of the parallel converters, with a dedicated task of VAR compensation of load at fundamental power frequency. The load harmonic currents are compensated by a parallel connected low power high frequency APF. Two types of parallel configurations have been investigated and compared for sharing of VAR support and load current harmonic elimination, so that the efficiency of the parallel load compensation scheme is maximized.

This study is useful for design of UPQC for high power application.

Chapter 6 summarizes the contributions of the dissertation, and gives suggestions for further research in this field.

Chapter 2

A Brief Survey on Major Custom Power Equipments and Their Control

---

2.1 Introduction

Power Quality (PQ) has been identified as an area of major concern for improving system efficiency, minimizing various losses, and ensuring production quality. To protect the interest of utility, international agencies like IEEE, IEC have been developing various standards for harmonic specifications for the Point of Common Coupling (PCC) as well as individual equipment. Power Quality surveys have been conducted to find out various effects of power disturbances on industrial production. As discussed in Chapter 1, voltage sag has been found out to be a major PQ disturbance for which industries suffer huge production loss in terms of material, manpower and money. No specific mandatory standards have come up yet to protect consumer interest from such utility voltage disturbance, though voltage distortion limits have been specified by standards. World wide research on custom power equipment is trying to develop suitable utility interface, which can protect both utility and interest of consumers.

In the present chapter, harmonic standards and specifications are discussed. Developments of various Power Quality Control measures, which are active solutions to various PQ issues, termed as *custom power equipments*, are reviewed.

2.2 International Agency Specification and Harmonic Standards

To prevent harmonic current flowing back to power system and affecting other loads at the Point of Common Coupling (PCC), limits of harmonic voltages and currents have been set by IEEE-519 standard [2].

The voltage distortion limits has been given in Table 2.1, where it is specified that utility voltage distortion should not exceed 5% at PCC voltage below 69 kV.

Table 2.1

IEEE 519 Voltage Limits

Bus Voltage	Maximum Individual Harmonic Components (%)	Maximum THD (%)
69kV and below	3	5
115kV to 161kV	1.5	2.5
Above 161kV	1	1.5

For power system below 69 kV, the harmonic current limits are listed in Table 2.2. Even harmonics are limited to 25% of odd harmonic limits. Stricter limits are applied to low short circuit ratio (SCR), which is defined as the ratio of maximum short circuit current, I_{sc}, and the average maximum monthly demand load current, I_L. All generation equipments need to use the strictest limits, i.e., SCR<20.

Table 2.2

IEEE 519 Current Limits

SCR = I_{sc}/I_L	h<11	11 to 17	17 to 23	23 to 35	35<h	THD
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

In Table 2.2, h is the harmonic number.

2.3 Research on Custom Power Equipments

The ongoing development of high power, high current and fast acting power semiconductor switching devices has revolutionized the area of Power Quality control. Today, every custom power technology, which can provide high control bandwidth and good controllability, involves power electronic converters. These converters are positioned depending upon the applications. For VAR support and load harmonic compensation, the converter is connected in *parallel* (*shunt*) to the load. These are broadly termed as Static VAR Compensator (**SVC**), Active Power Filter (**APF**), or Synchronous Link Converter VAR Compensator (**SLCVC**). For voltage support to the load end, the connection of converter is such that it can inject voltage in *series* with the utility. This class of equipments is termed as Dynamic Voltage Restorer (**DVR**).

A third category of custom power equipment has been developed which is a combination of *series and shunt* compensators. They are termed as Unified Power Quality Conditioners (**UPQC**) [15-18].

Various custom power equipments have been developed depending upon power circuit topology and position of the converters. The classification of custom power equipments are given in Fig. 2.1. In the following sections, the details of power circuit topologies and their functions are reviewed.

All these power semiconductor devices need to be controlled fast, so detection algorithms are also important for effective on-line closed-loop control. Several detection methods to generate reference signals have also been discussed.

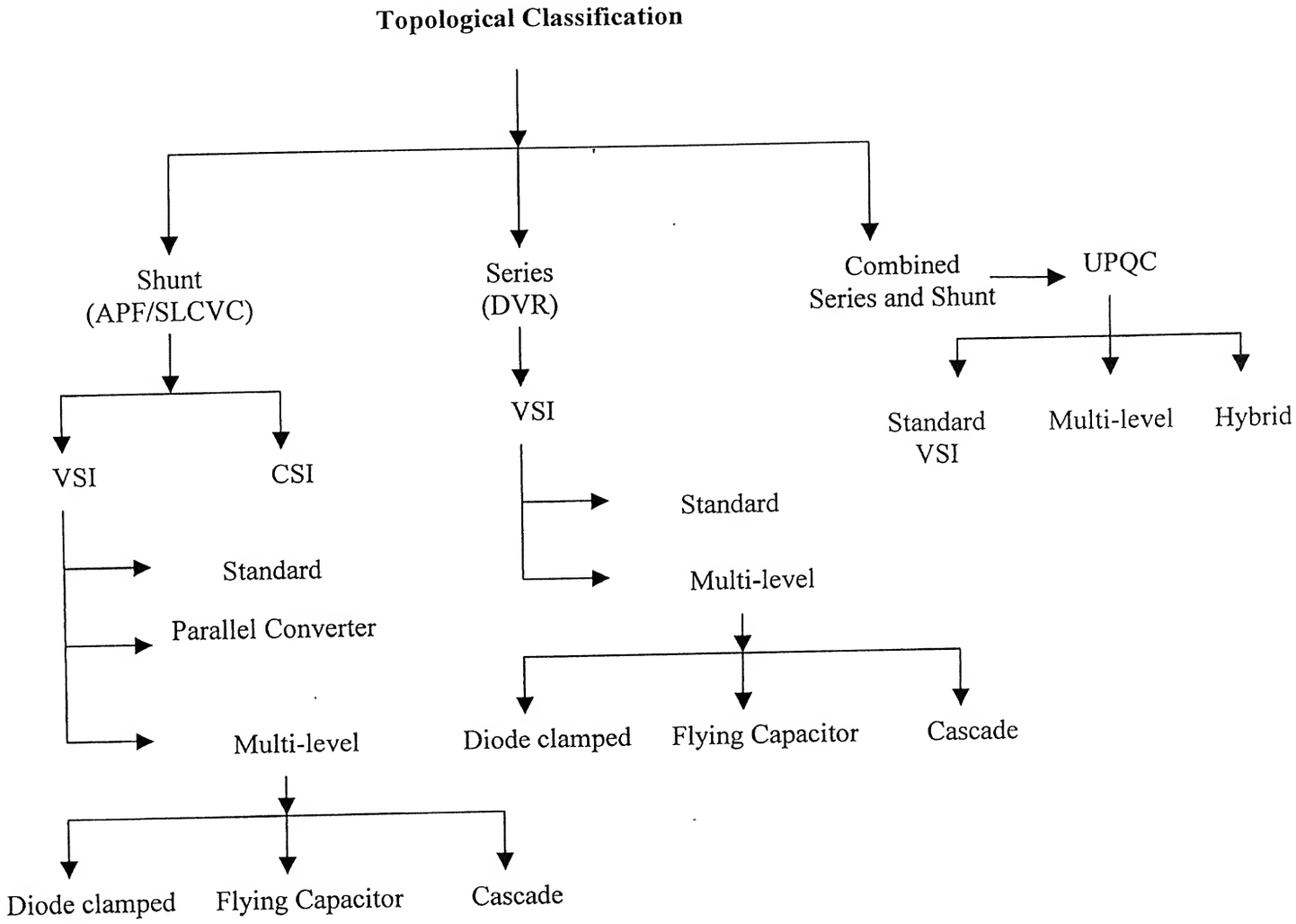

Fig. 2.1 Classification of Power Quality Conditioners

2.3.1 Active Power Filter (APF) / Synchronous Link Converter VAR Compensators (SLCVC)

The research in Power Quality Control for load compensation started with Static VAR Compensator (SVC) and Active Power Filtering, with different converter topology (e.g. VSI, CSI, Parallel, Multilevel etc.) and control strategy [19-33]. The converters are connected in parallel to the load. These converters generate non-linearity in a sense opposite to the load non-linearity. As the load harmonics are eliminated by controlling the device switching instants, the harmonic compensation can be on-line.

The main features of this class of equipments are as follows

1. Reactive power compensation capability is independent of absolute magnitude of the terminal voltage but on the difference between the fundamental inverter input voltage (V_{c1}) (dependent of the dc link voltage Vdc) and the utility voltage (V_s) according to the following equation,

$$Q = \frac{V_s|V_s - V_{c1}|}{\omega L_{SLC}} \qquad (2.1)$$

where, Q is the reactive power of the load, L_{SLC} is the value of synchronous link inductance and ω corresponds to the fundamental angular power frequency.

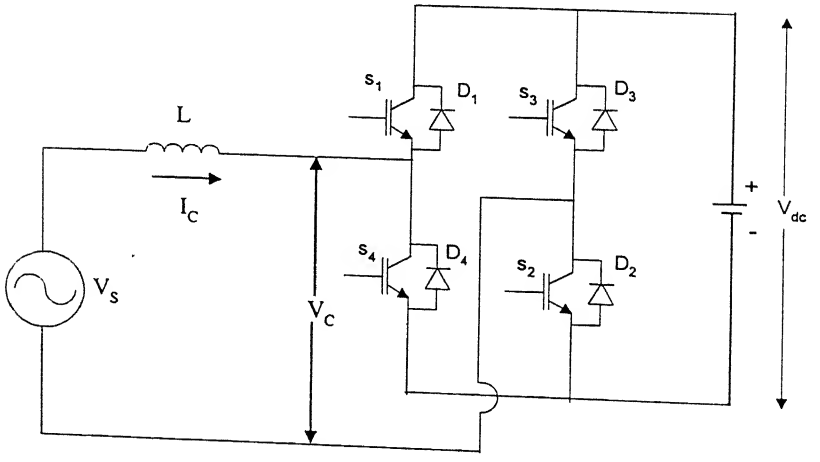

Fig. 2.2 A single phase SLCVC connection with supply

2. As non-linear switching action is used to generate the VAR, and suppress harmonics, theoretically no energy storing passive element is required, therefore there will be low system losses and high efficiency.
3. Due to fast acting switches, these converters can cover wide bandwidth for harmonic elimination.

The most popular converter topology which have been reported are three phase three wire and three phase four wire (neutral connected) topologies with hard switching [19-25]. A dc link capacitor is used as a dc voltage source, and an inductor at the output of the inverter to the PCC to control the current flow. These converters are suitable for low-medium power applications where fast switching is possible and the switching techniques are mostly based on current control [19-21, 25-28], which helps to eliminate the undesirable harmonics from the supply. The deviation of dc link voltage from its reference gives a measure of the active component of current requirement from the supply. Based on this error, the magnitude of supply current reference can be determined. In many applications, the unbalancing in the load currents is nullified by controlling the neutral wire current [28-29].

For high power applications where high current puts limit to the switching frequency, the converters are operated in voltage controlled mode. By adding more number of parallel modules with appropriate phase shift introduced, the rating of the converter can be increased [30]. The other viable option is to use multilevel inverters [31-33].

Parallel converter scheme

Parallel converter scheme is used for high power application. The scheme reported in [30] has eight three phase transformers with additional phase shift winding along with each primary winding as shown in Fig. 2.3. Each secondary winding of the transformer is connected to a full bridge converter. All the converters are connected in parallel on dc side to a single capacitor bank. Converter output voltages corresponding to each phase are shifted by 7.5°. On primary side of the transformers, main winding of each phase is connected to the phase shift winding in the next phase with polarities opposing each other. This adds the phase winding voltage at 120° to the main winding voltage. By choosing

appropriate turns ratio, vector addition of the two voltages are maintained constant in such a way that

(i) it compensates for converter phase shift of 7.5°.

(ii) phase voltage generated by each winding adds to develop a 48-pulse phase voltage waveforms at source terminals. The phase voltage is quite close to a sinusoid and develops only 48±1 current harmonics.

The following disadvantages are also associated with this parallel converters scheme

- A number of transformers are required, which increases the overall weight, cost and size.
- Performance to cost ratio decreases as number of parallel units increases with the increase in number of harmonics to be eliminated.
- Control structure is complicated and a good co-ordination is required.

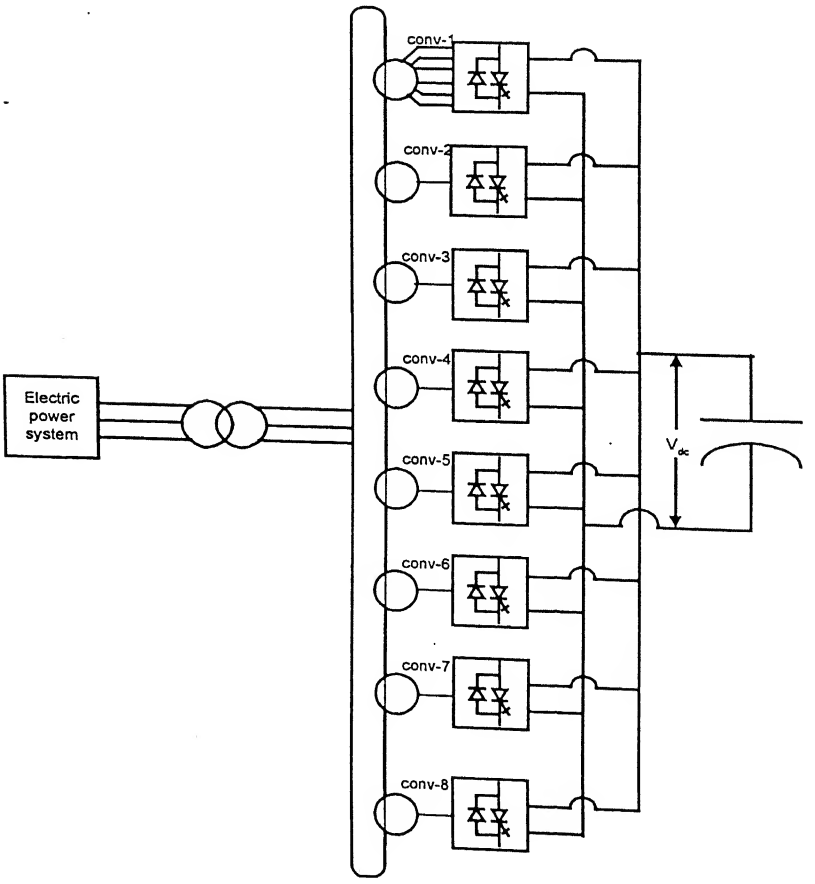

Fig. 2.3 Parallel converter scheme

Multilevel Converters

The multilevel voltage source inverter has been recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, UPQC, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [31-33]. The output voltage waveform of a multilevel inverter is composed of the number of voltage levels, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints.

- The voltage capacity of the existing devices can be increased many times without the complications of static and dynamic voltage sharing that occur in series-connected devices.
- Spectral performance of multilevel waveforms is superior to that of their two-level counter-parts.

The three major configurations of multilevel converters [33] are
Diode Clamped multilevel inverter (DCMI)
Flying Capacitor multilevel inverter (FCMI)
Cascaded Inverter with separate dc source.

Out of these three configurations, diode-clamped converters have been more widely investigated. DCMI uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m-level diode-clamped inverter needs m-1 capacitors on the dc bus. A three-phase five-level diode-clamped inverter is shown in Fig. 2.4. The dc bus consists of four capacitors, i.e., C_1, C_2, C_3, and C_4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes. DCMI output voltage synthesis is relatively straightforward. To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage

reference point. For the five-level inverter shown in Fig. 2.4, there are five switch combinations to generate five level voltages across A and O. Table 2.3 shows the phase voltage levels and their corresponding switch states.

In Table 2.3, Switch-state 1 indicates that the switch is on, and Switch-state 0 indicates that the switch is off. In each phase leg, a set of four adjacent switches is on at any given time. There exist four complementary switch pairs in each phase, viz., S_{a1}-$S_{a'1}$, S_{a2}-$S_{a'2}$, S_{a3}-$S_{a'3}$ and S_{a4}-$S_{a'4}$ for phase –A. Similar switch pairs can be found out for phases B and C.

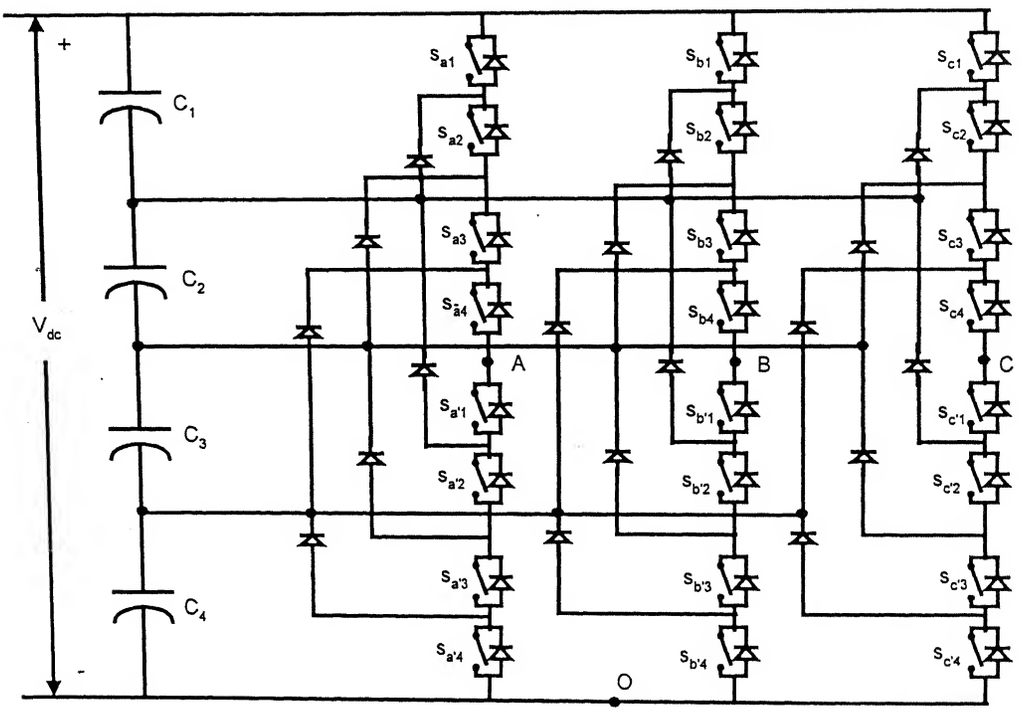

Fig.2.4 Three phase five-level DCMI

Table 2.3 Diode-clamped five-level inverter voltage levels and their switch states.								
Output	Switch State							
V_{AO}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

Flying Capacitor Multilevel Inverter (FCMI)

The power circuit of a three phase, five level FCMI is shown in Fig. 2.5. It is proposed as an alternative to diode clamped topology. The significant advantage of this topology is that it eliminates clamping diode problems present in the diode clamped multilevel topologies. Additionally, this topology naturally limits the dv/dt stress across the devices and introduces additional switching states that can be used to help maintain the charge balance in the capacitors. Also, flying capacitor topology has enough redundant switching states to control the charge balance in the single isolated leg with converters having any number of levels, even if the phase current is unidirectional.

Disadvantages:

The dc link charge controller adds complexity to the control of whole circuit.

The flying capacitor topology requires more capacitance than the equivalent diode clamped topology. It is also obvious that rather large rms currents will flow through these capacitors. A study of the trade-offs involved is not described in the available literature.

There is potential parasitic resonance between decoupling capacitors. Table 2.4 shows a possible switching state for the five-level flying capacitor topology given in Fig. 2.5.

Table 2.4 A possible switch combination of the voltage levels and their corresponding switch states of Five-level Flying Capacitor Inverter

Output V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

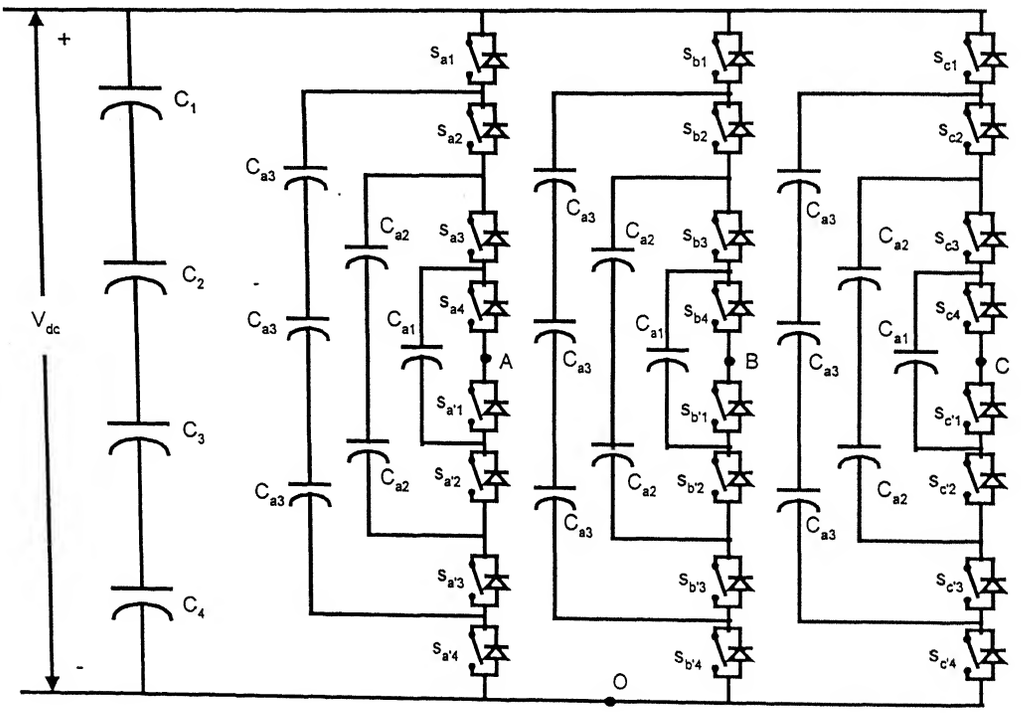

Fig. 2.5 Three phase five-level FCMI

Cascaded Inverter with separate dc source

The power circuit of one phase of a n-level cascaded inverter with separate dc source is shown in Fig. 2.6. The primary advantage of the topology is that increase in number of level is possible without introducing complexity in the power stage. With increase in

power level, the numbers of switches required are same as diode clamped topology, but extra clamping diodes are not required. Modularity of the topology is preferred and considered as advantage in many applications, but separate dc sources are required.

In high power application, multilevel inverters are viable alternatives without the need of transformers. All topology can be used for reactive power compensation. However, the voltage balancing problem needs special attention. As the number of components increase with number of levels, control also becomes complex.

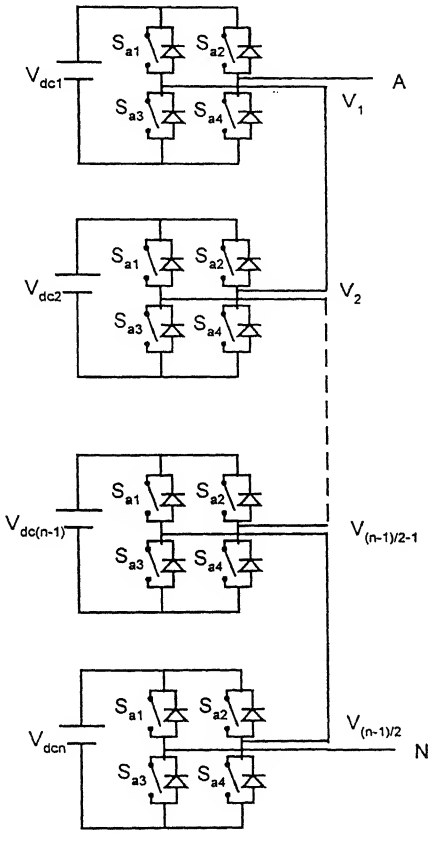

Fig. 2.6 Single-phase structure of a multilevel cascaded inverter

2.3.1.1 Detection algorithms

The performance of shunt filter depends upon many factors. Among them, reference current generation is the most important. The three basic theories developed for detection and estimation of reference generation are Instantaneous Reactive Power (IRP) Theory

[34, 35], Synchronous Reference Frame (SRF) Theory [36], and Sequence Component Analysis (SQA) [37-38].

2.3.1.1a Instantaneous Reactive Power (IRP) method

Akagi introduced the IRP theory [34]. This technique is suitable for three phase systems. The instantaneous power of the load is calculated. It consists of a dc component and an oscillating component. The oscillating component, which is due to unbalance and load harmonics, is separated over a certain interval of time (an integral number of cycles). In order to obtain the reference currents according to this theory, three-phase voltages (v_a, v_b, v_c) and currents (i_a, i_b, i_c) are first transformed to α-β system, using the following equations.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.2}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.3}$$

Then instantaneous active power 'p' and instantaneous reactive power 'q' are defined as

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.4}$$

$$p = v_\alpha * i_\alpha + v_\beta * i_\beta = \mathrm{P} + \tilde{\mathrm{p}} \tag{2.5}$$

$$q = v_\alpha * i_\beta - v_\beta * i_\alpha = \mathrm{Q} + \tilde{\mathrm{q}} \tag{2.6}$$

According to IRP theory, 'p' describes the instantaneous active three phase power and 'q' consists of all portions of phase powers that do not contribute to the instantaneous

active three phase power. P and Q are average values of active and reactive power and $\tilde{p}$, $\tilde{q}$ are ac quantities of active and reactive power of p and q respectively.

When the load is linear and balanced, and the supply is also balanced, p and q only contain dc components.

If the active filter is to compensate for load harmonic and negative sequence current. the reference currents for the compensator can be calculated as follows.

$$\begin{bmatrix} i^*_{c\alpha} \\ i^*_{c\beta} \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} -\tilde{p} + P_{Loss} \\ -\tilde{q} \end{bmatrix} \qquad (2.7)$$

The currents are next transformed back to three phase system by the following equation

$$\begin{bmatrix} i^*_{ca} \\ i^*_{cb} \\ i^*_{cc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i^*_{c\alpha} \\ i^*_{c\beta} \end{bmatrix} \qquad (2.8)$$

P_{Loss} is the power corresponding to the loss component of the converter system and i_{ca}^*, i_{cb}^* and i_{cc}^* are references for compensator currents.

This scheme is most widely used in literature because of its flexibility and fast dynamic response. At the same time the calculation is quite complex and the inherent assumption is that the supply is balanced.

2.3.1.1b Synchronous Reference Frame (SRF) based algorithm

The method proposed by Bhattacharya [36] is based on the calculation of the i_d^e-i_q^e components of the instantaneous three-phase currents in a synchronously rotating reference frame, which rotates synchronously with the voltage phasor. The synchronous reference angle comes from a phase locked loop (PLL). In this rotating reference frame,

the fundamental component of a-b-c frame currents are transformed to dc levels in i_d^e-i_q^e currents, which are filtered by conventional filters.

If the currents are balanced and sinusoidal, i_d^e and i_q^e will be dc quantities. However, in the presence of harmonics and unbalanced load current, the d^e-q^e currents contains an ac components in addition to the dc components.

The abc-dqo and dqo-abc transformation matrices are given below.

$$\begin{bmatrix} v_q^e \\ v_d^e \\ v_o^e \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(wt+\alpha) & \cos(wt-\frac{2\pi}{3}+\alpha) & \cos(wt+\frac{2\pi}{3}+\alpha) \\ \sin(wt+\alpha) & \sin(wt-\frac{2\pi}{3}+\alpha) & \sin(wt+\frac{2\pi}{3}+\alpha) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \qquad (2.9)$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(wt+\alpha) & \sin(wt+\alpha) & \frac{1}{\sqrt{2}} \\ \cos(wt-\frac{2\pi}{3}+\alpha) & \sin(wt-\frac{2\pi}{3}+\alpha) & \frac{1}{\sqrt{2}} \\ \cos(wt+\frac{2\pi}{3}+\alpha) & \sin(wt+\frac{2\pi}{3}+\alpha) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_q^e \\ v_d^e \\ v_o^e \end{bmatrix} \qquad (2.10)$$

The d^e-q^e voltage/current components are suitably filtered and processed to obtain the reference compensator signals in d^e-q^e frame. The variables in d^e-q^e frame are converted back into abc frame for actual implementation.

This method is immune to the presence of harmonics in the voltages, once the PLL presents a strong characteristic of noise rejection. The method uses conventional filters, so it has also a slow transient response.

2.3.1.1c Sequence Component Analysis (SQA)

The theory of symmetrical components can be used for the purpose of load balancing, harmonic suppression and power factor correction. Algorithms provided by this theory can

practically compensate any kind of harmonics and unbalance in the load provided a high band width current source to track the filter reference currents is available.

The compensation scheme can be applied to three phase three wire or three phase four wire system such that the supply current is balanced with no zero sequence components.

Let us take an example of a three phase three wire system as shown in Fig. 2.7 [38]. It is desired that the supply current should be balanced and sinusoidal.

Therefore,

$$i_{sa} + i_{sb} + i_{sc} = 0 \tag{2.11}$$

From power factor consideration, we assume that phase of the vector i_{sa1} lags that of v_{sa1} by an angle ϕ, i.e.,

$$\angle\{v_{sa} + av_{sb} + a^2 v_{sc}\} = \angle\{i_{sa} + ai_{sb} + a^2 i_{sc}\} + \phi, \tag{2.12}$$

where, $a = e^{j120^o}$. Substituting the values of a and a^2, (2.12) can be expanded as

$$\angle\left\{\left(v_{sa} - \frac{1}{2}v_{sb} - \frac{1}{2}v_{sc}\right) - j\frac{\sqrt{3}}{2}(v_{sb} - v_{sc})\right\} = \angle\left\{\left(i_{sa} - \frac{1}{2}i_{sb} - \frac{1}{2}i_{sc}\right) - j\frac{\sqrt{3}}{2}(i_{sb} - i_{sc}) + \phi\right\} \tag{2.13}$$

Equating the angles, we can write from the above equation

$$\tan^{-1}\left(K_1 / K_2\right) = \tan^{-1}\left(K_3 / K_4\right) + \phi \tag{2.14}$$

where,

$$K_1 = \frac{\sqrt{3}}{2}(v_{sb} - v_{sc}), K_2 = v_{sa} - \frac{1}{2}v_{sb} - \frac{1}{2}v_{sc}, K_3 = \frac{\sqrt{3}}{2}(i_{sb} - i_{sc}) \text{ and } K_4 = i_{sa} - \frac{i_{sb}}{2} - \frac{i_{sc}}{2} \tag{2.15}$$

Taking tangent of both sides of (2.14), we get

$$\frac{K_1}{K_2} = \tan\left[\tan^{-1}\left(K_3 / K_4\right) + \phi\right] \tag{2.16}$$

Substituting the values of K_1 to K_4 in (2.16), we get

$$(v_{sb} - v_{sc} - 3\beta v_{sa})i_{sa} + (v_{sc} - v_{sa} - 3\beta v_{sb})i_{sb} + (v_{sa} - v_{sb} - 3\beta v_{sc})i_{sc} = 0 \tag{2.17}$$

where, $\beta \equiv \tan\phi/\sqrt{3}$.

The compensator is required to supply the reactive current, the negative sequence currents and the harmonic currents. The source supplies the average value of the load power P_{L_avg}.

$$P_{L\_avg} = v_{sa}i_{sa} + v_{sb}i_{sb} + v_{sc}i_{sc} \tag{2.18}$$

The average load power P_{L_avg} may be computed by using a moving average filter that has an averaging time of half a cycle. It is to be noted that any harmonic component in the load does not require any real power from the source. The equation (2.18) holds good even when the load current contains harmonics or is non-periodic.

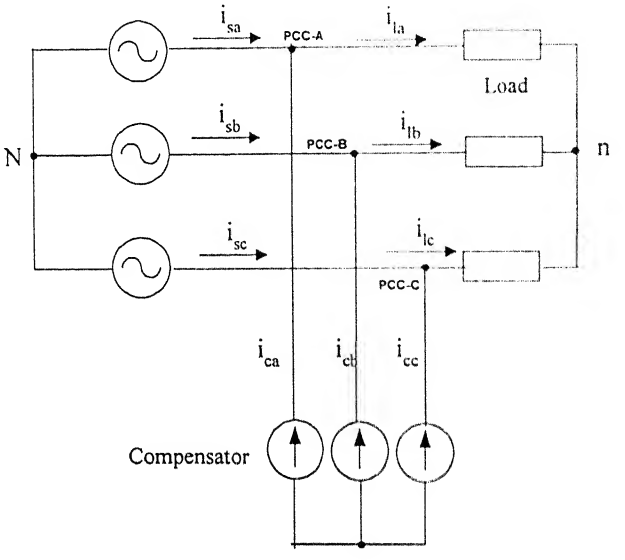

Fig. 2.7 Schematic diagram of the compensation scheme for star connected load and 3-wire supply

From (2.11), (2.17) and (2.18)

We get

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ (v_{sb} - v_{sc} - 3\beta v_{sa}) & (v_{sc} - v_{sa} - 3\beta v_{sb}) & (v_{sa} - v_{sb} - 3\beta v_{sc}) \\ v_{sa} & v_{sb} & v_{sc} \end{bmatrix}^{-1} \begin{bmatrix} 0 \\ 0 \\ P_{L\_avg} \end{bmatrix} \quad (2.19)$$

From Fig.2.7 applying KCL at PCC, we get

$$i_{sa} = i_{la} - i^*_{ca}, i_{sb} = i_{lb} - i^*_{cb}, i_{sc} = i_{lc} - i^*_{cc} \quad (2.20)$$

From (2.19) and (2.20) we can write

$$\left.\begin{aligned} i^{*}_{ca} &= i_{la} - \frac{(v_{sa}-v_{so})+\beta(v_{sb}-v_{sc})}{\Delta} P_{L\_avg} \\ i^{*}_{cb} &= i_{lb} - \frac{(v_{sb}-v_{so})+\beta(v_{sc}-v_{sa})}{\Delta} P_{L\_avg} \\ i^{*}_{cc} &= i_{lc} - \frac{(v_{sc}-v_{so})+\beta(v_{sa}-v_{sb})}{\Delta} P_{L\_avg} \end{aligned}\right\} \quad (2.21)$$

where,

$$v_{so} = \frac{1}{3}\sum_{j=a,b,c} v_{sj} \quad and \quad \Delta = \sum_{j=a,b,c} v_{sj}^2 - 3v_{so}^2 . \quad (2.22)$$

For balanced supply v_{so}= 0. Therefore, reference compensator currents in (2.21) reduces to

$$\left.\begin{aligned} i^{*}_{ca} &= i_{la} - \frac{v_{sa}+\beta(v_{sb}-v_{sc})}{\Delta} P_{L\_avg} \\ i^{*}_{cb} &= i_{lb} - \frac{v_{sb}+\beta(v_{sc}-v_{sa})}{\Delta} P_{L\_avg} \\ i^{*}_{cc} &= i_{lc} - \frac{v_{sc}+\beta(v_{sa}-v_{sb})}{\Delta} P_{L\_avg} \end{aligned}\right\} \quad (2.24)$$

When the compensator compensates for load reactive power in addition to negative sequence and harmonic currents, β in (2.24) can be made zero. Therefore, compensator currents obtained in (2.24) can be impressed in the actual system by having a high bandwidth current controller.

2.3.2 Series Compensator/Dynamic Voltage Restorer (DVR)

To protect the voltage sensitive loads and sophisticated control equipments from supply voltage sag and other disturbances, the research in the area of DVR has progressed. But it does not have any influence on load current harmonic elimination.

The most likely causes of voltage sag are given as follows [39, 40]

- Sudden loading of the system at PCC, as in the case of Direct On Line (DOL) start of Induction motor.
- Sustained faults not cleared due to failure of primary protection schemes.

- Improper grounding
- Large neutral currents due to unbalanced loading
- Poor transformer regulation due to internal faults.

As observed from PQ survey voltage sag is the primary disturbance for customers and DVR is used to attend this problem.

The heart of the DVR is a standard VSI, but different control strategy makes its performance different. An AC chopper based DVR has been proposed in [40] as shown in Fig. 2.8. A booster transformer is connected in series with the voltage sensitive load. The secondary of the transformer injects suitable corrective voltage in a feed forward manner. The dc voltage of the chopper is supplied from an UPS.

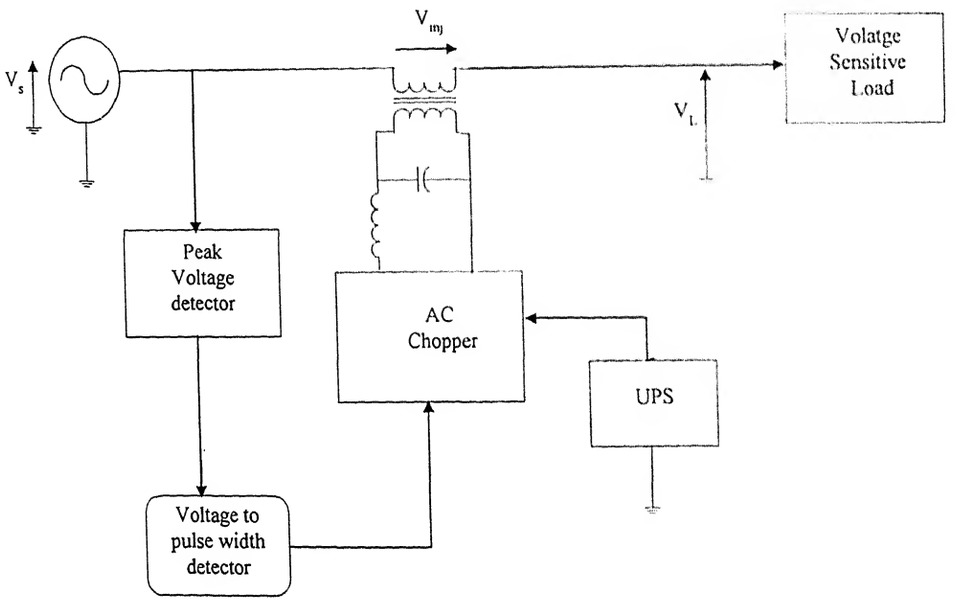

Fig. 2.8 A scheme of voltage sag compensation

Three techniques of DVR compensation [41, 42] are discussed below.

1. Reactive Power Compensation Technology:

Here injected voltage (V_{dvr}) is in quadrature with load current, so the DVR does not consume any real power as seen from phasor diagram of Fig. 2.9a. The relationship amongst various voltages is given by

$$V_S^2 = V_L^2 - 2V_L V_{dvr} \sin\Phi + V_{dvr}^2 \qquad (2.13)$$

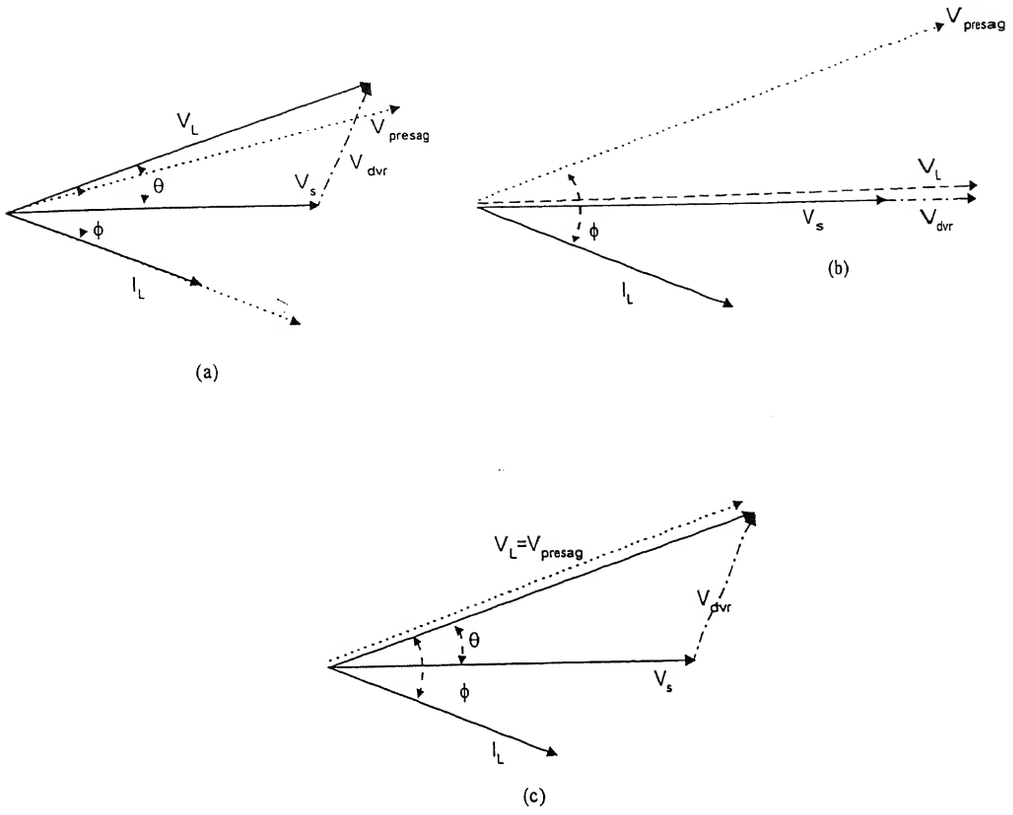

Fig. 2.9 Phasor diagrams for different DVR schemes

2. In-phase Compensation:

Here the boost voltage is in phase with supply voltage as seen in Fig. 2.9b. The DVR handles both active and reactive power.

3. Phase cum magnitude compensation:

The control scheme for both magnitude and phase compensation (Fig. 2.9c) has been reported is discussed in [42]. A PLL tracks the phase angle of the positive sequence voltage of the supply and acts as the multiplying angle for the rotating d-q fraime, such that the phase angle information is always that of the supply. In the d-q reference frame, the d-axis reference is made equal to the balanced nominal voltage and q- axis reference is set zero. The supply voltages are also converted to d-q reference frame and compared with

the reference. The error voltage is converted back into 3 phase co-ordinate systems and the DVR converter supplies the series voltage to be injected. The control is open loop in nature.

Simulation of type-1 has been investigated in [43, 44] and type-2 method of sag compensation is carried out in [41]. The performances of type-1 and type-2 methods have been compared.

The filter used after the DVR for high frequency harmonic filtering introduces phase shift, and affects both the dynamic and steady state response. Filters can be used in the inverter side or in the line side as shown in Fig. 2.10. However, a careful design of the filter and the control circuit has to be made to obtain good control response [43, 45].

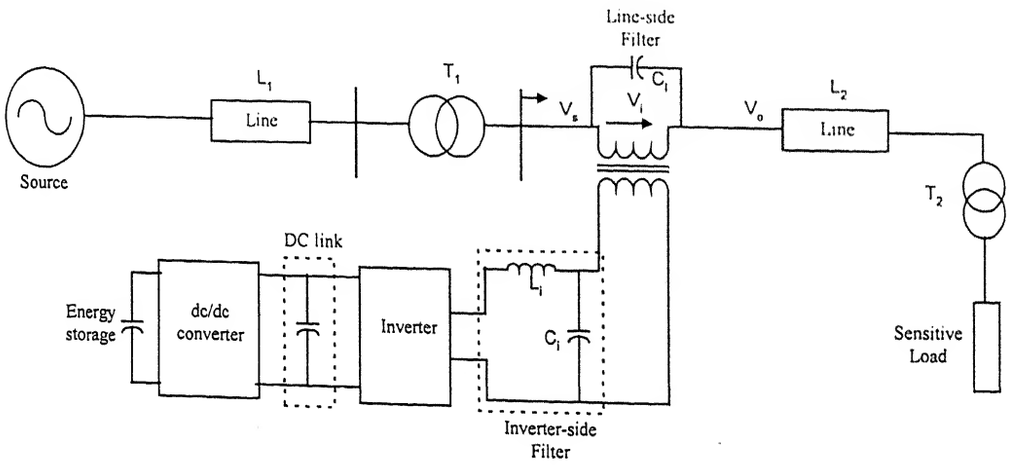

Fig. 2.10 Possible filtering scheme in DVR

Special design considerations for DVR are described in [45, 46], which are noted below.

- DVR must lock into the supply phase and must detect the supply voltage reduction accurately.
- During restoration, the dc link voltage should be maintained at a certain level to ensure proper injection
- As PWM scheme is used to synthesize the injected voltage, the switching frequency harmonics must be prevented from entering into the utility and customer system. A Low Pass Filter (LPF) must be introduced to accomplish this function. However, there will be an additional voltage drop when the load current flows through filter.

Most DVR control schemes provide feed-forward control to have fast dynamic response and small static error. A state feedback closed-loop control scheme has been proposed by the authors [45, 46] to ensure effective voltage injection.

A useful comparative study of the position of filters in DVR has been reported in [45].

Advantages of inverter side filter (Fig. 2.10)

- It is on the low voltage side of the transformer
- It is close to the harmonic source
- Using this scheme, the high order harmonic currents will be prevented from penetrating into the series transformer

Disadvantages

- When DVR acts as a source, the introduction of filter inductor L_1, may cause the voltage drop and phase angle shift in the fundamental component of inverter output.
- As DVR is a series device, inductor may also cause a drop in the distribution system supply voltage

Though the disadvantages can be eliminated in line side filtering, the harmonic currents will flow into the injection transformer and its rating has to be increased.

2.3.3 Unified Power Quality Conditioner (UPQC)

The third category of custom power equipment being developed is Unified Power Quality Conditioners (UPQC), which addresses to both voltage and current quality issues, and protects both utility and consumer interests with a suitable combination of series and shunt compensators. In 1996, H. Akagi proposed the term Unified Power Quality Conditioner (UPQC) [15] for distribution system.

The idea of combining series and shunt compensator for effective power flow control in transmission system was first proposed by L. Gyugyi in 1991 [48]. He used the term,

Unified Power Flow Controller (UPFC) [49]. But the relative placing of the compensators and their respective performance objective were different [50-52].

Primarily, UPFC has shunt inverter nearer to the source. It is operated in such a way as to draw a controlled current from the ac bus. The current reference is chosen to satisfy the shunt reactive power reference and to provide any real power needed to balance the real power of the series inverter. A small amount of real power is also drawn to cover the power losses of the inverter and magnetics. The shunt reactive power reference can be either capacitive or inductive. The series inverter controls the magnitude and angle of the voltage injected in series with the line. The voltage injection is always intended to influence the flow of power on the line.

There are a few publications about combining active series compensator with passive shunt compensator [53-55]. Very few publications are available till date on UPQC reporting experimental realization. Some typical available literatures on UPQC are discussed here.

M. Aredes et al. (1998) reported the simulated performance of a Unified Active Power Line Conditioner (UPLC) for nonlinear three phase four wire load, with split capacitor topology [56] (Fig. 2.11).

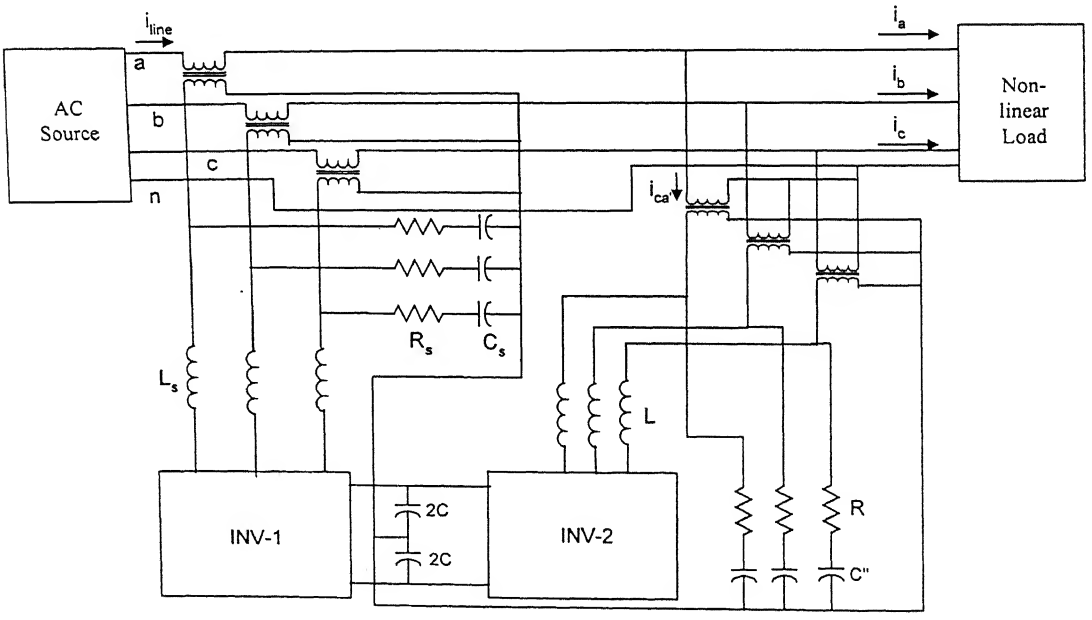

Fig. 2.11 Power circuit configuration of UPLC for a three phase four wire system

The scheme simultaneously aimed at active power flow control, load reactive power compensation, voltage regulation and harmonic isolation. The control schemes used α-β

reference frame theory to extract the positive sequence voltage and current with the help of a PLL. The digital simulation results are reported. However, the control scheme is of formidable complexity and simplification of control objectives is required to arrive at a economically viable scheme.

In [57], the authors have reported some work on UPQC for low frequency flicker balance in supply voltage. The shunt and series converter positions are opposite to the conventional UPQC [53, 56]. The shunt converter is connected near to the utility. The shunt converter is a three phase PWM-VSI that only maintains the dc link voltage between the two converters. Though it has capacity to compensate for the reactive power of the load, it is not assigned that duty. A passive filter (5^{th}, 7^{th} and HP Filter) is installed near the load to compensate for the harmonics produced by the load. The series converter, which is installed after the shunt active filter and shunt passive filter, is a combination of three single phase H-bridge IGBT inverters. With the help of IRP theory, the series filter injects similar frequency voltage as that of the supply flicker, but in the opposite sign. Therefore, the supply voltage flicker cancels out leading to a flicker-less load voltage. However, as the VAR requirement of the load was not compensated, so the supply voltage and current would not be in phase in case of a reactive load. It is also not applicable for a single phase load.

A tri-level inverter (Fig.2.12) with dual DSP control is investigated with synchronous A/D sampling technology [58]. Here, a battery energy storage unit is used to maintain the dc link balance between the two dc capacitors of the tri-level inverter, and acts as a stand by generator. The switching instants are generated by space vector modulation technique and a digital dead bit control is used for reactive power compensation.

Two DSPs are engaged in controlling the UPQC. DSP-1 generates the reference voltage for series injection and reference current for shunt compensation. DSP-2 generates the pulses to drive the IGBTs of the inverters. Both power circuit and control circuits are complex.

Elmitwally et al. [59] proposed a Fuzzy controller based algorithm for UPQC, which they termed as Power Quality Manager. The power circuit configuration is the same as shown in Fig. 2.11. The series reference voltage generator is shown in Fig. 2.13.

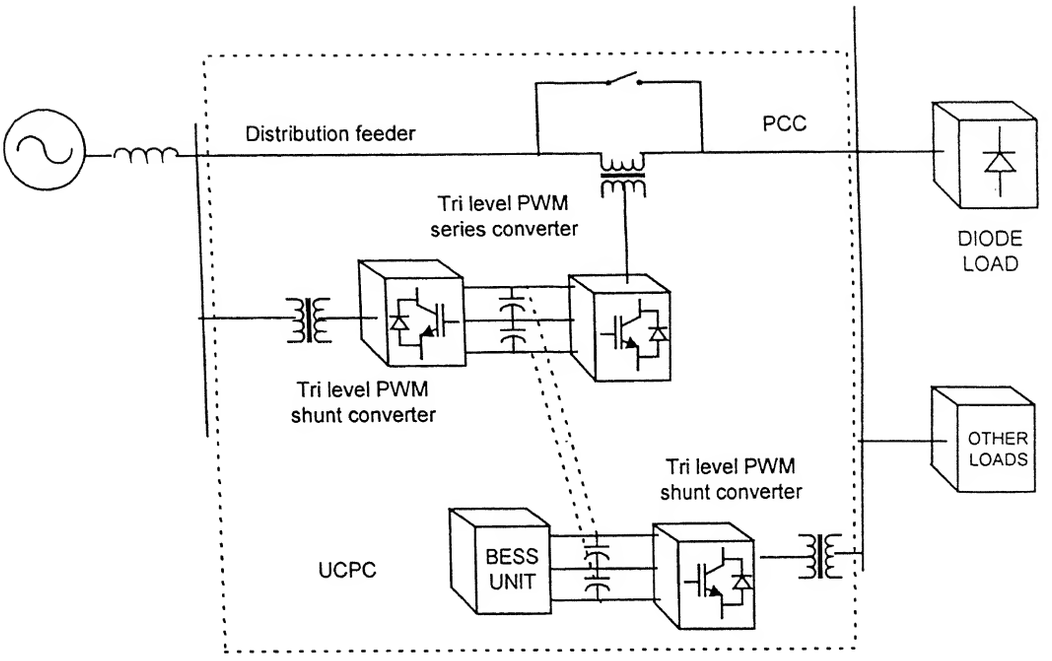

Fig.2.12 Power circuit of the proposed UPQC

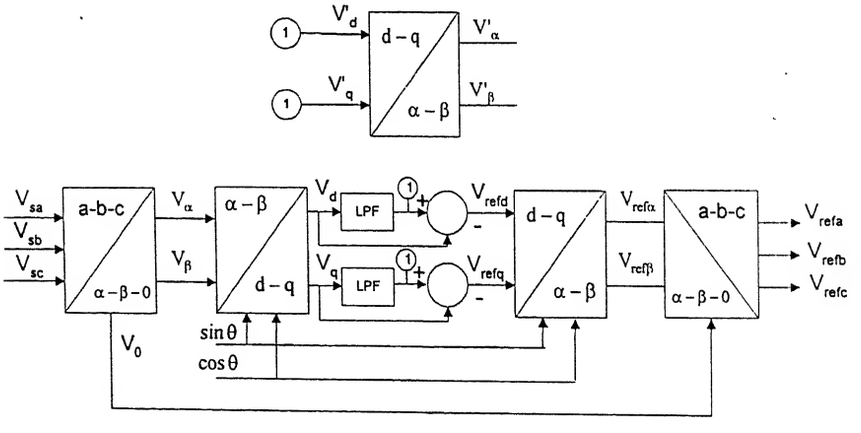

Fig.2.13 Reference voltage detection for the series converter

θ is a time varying angle that represents the angular position of the reference frame, which rotates at a constant speed in synchronism with the 3 phase ac voltages, and fundamental frequency components are converted to non-dc quantities.

Isolating fundamental component is done by a High Pass Filter (HPF), a 3rd order Butterworth filter, with a cut-in 25 Hz. Blocking of dc quantity by HPF provides insensitivity to phase errors (Fig. 2.13). This is an advantage of using SRF based control.

Voltage regulation control loop: The dc link voltage regulation loop is achieved by the shunt converter as shown in Fig. 2.14. A current signal, which accounts for the variation in RMS value of the fundamental load voltage, is superimposed on d-axis component of the load current. Two inputs, namely input current error '*e*', and change in current error '*Δe*' are required for the fuzzy controller (Fig. 2.14).

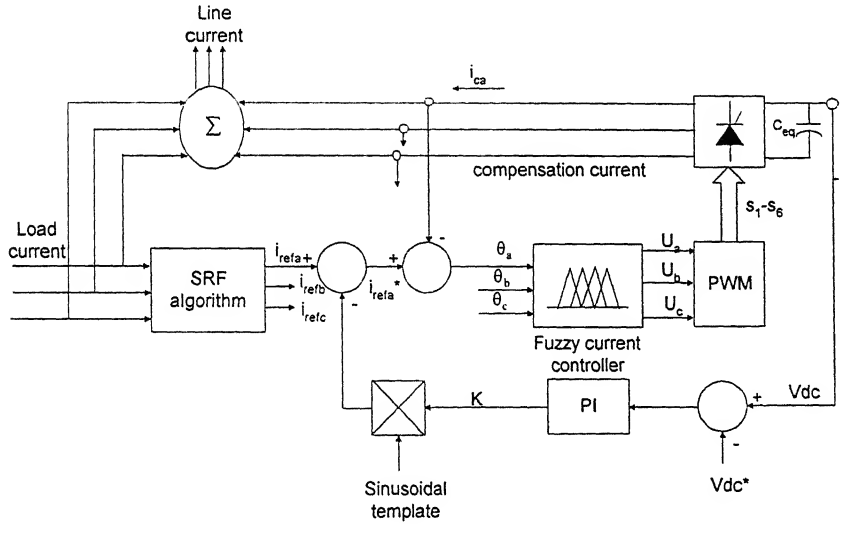

Fig.2.14 Current control of the shunt converter

The output gives switching functions for the shunt converter. Membership functions are triangular with 50 % overlap for a soft and progressive adjustment.

Li et al. [60] reported a hybrid UPQC scheme with passive filter (Fig. 2.15). The objectives are to eliminate the negative sequence harmonic components with some voltage by a series converter. The shunt converter is used for load reactive and harmonic current compensation. The passive filters are used for harmonic filtering in addition to power

factor correction. A constant sine wave is assigned for the load voltage reference. The distortion imbalance, sag flicker are corrected.

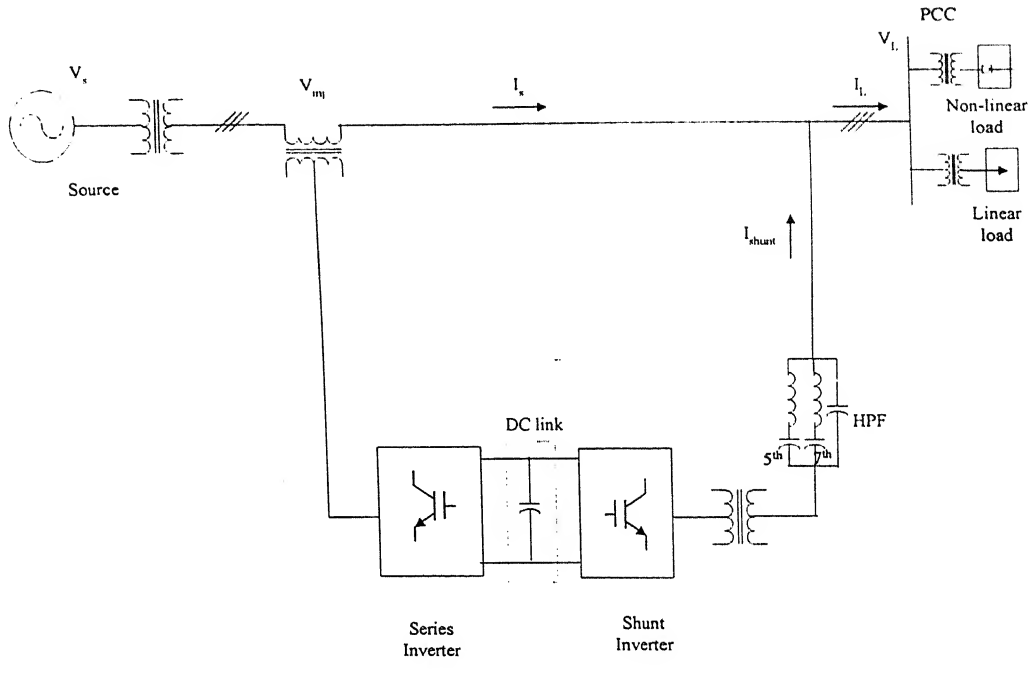

Fig. 2.15 Power circuit configuration of proposed hybrid UPQC

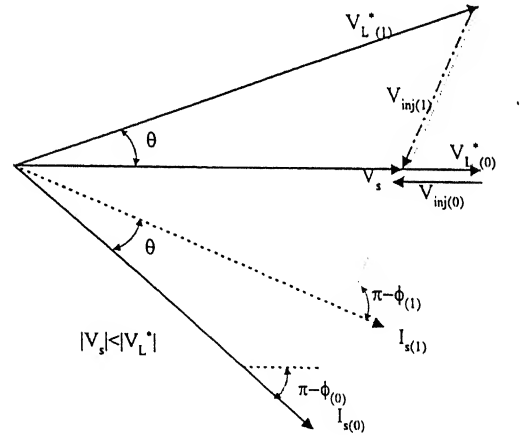

Fig. 2.16 Phasor diagram for voltage compensation

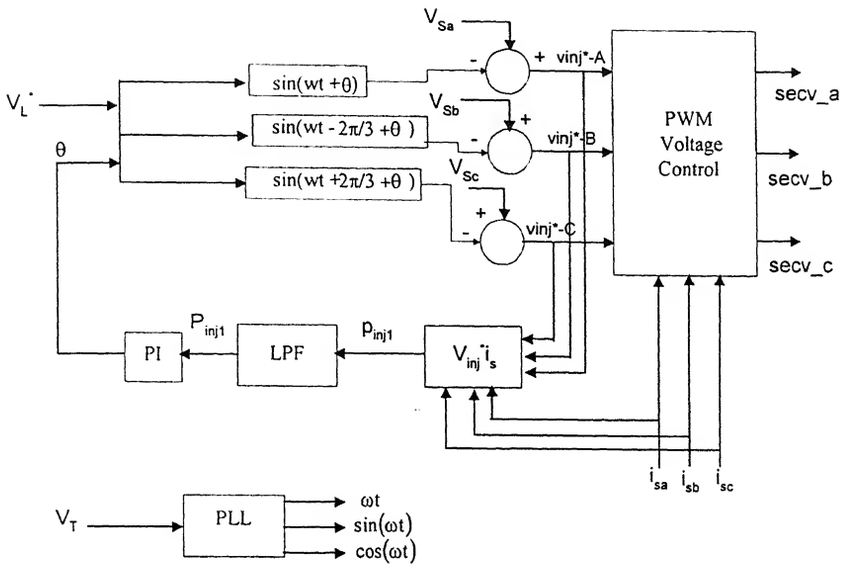

Fig. 2.17 Control logic for series active filter

By phase control of voltage reference (Fig. 2.16), series active filter can inject a fundamental voltage in quadrature with line current to maintain the voltage level without consuming energy. The control block diagram for the series active filter [60] is shown in Fig. 2.17.

The parallel filter is connected in series with a passive filter and controlled as a current source. Reference signal is extracted from the load current of the feeder. But, the open loop control cannot ensure zero error. The disturbances from both sides are isolated. The angle θ is regulated from the sign of power of active filter (series) so that sag/swell can be compensated. The d-q-o transformation is adopted for the shunt compensation.

A 6-level DCMI based Multilevel Unified Power Conditioner (MUPC) (Fig. 2.18) has been reported in [61]. The phase voltage synchronizing signals have been derived from the line voltages. Two kinds of modulation have been applied. For low modulation index (MI), a novel carrier rotation technique has been used to maintain the balanced device usage. For high MI, Switching Frequency Optimal PWM (SFO-PWM) has been applied. Generalized p-q theory has been applied for load current compensation by the parallel converter.

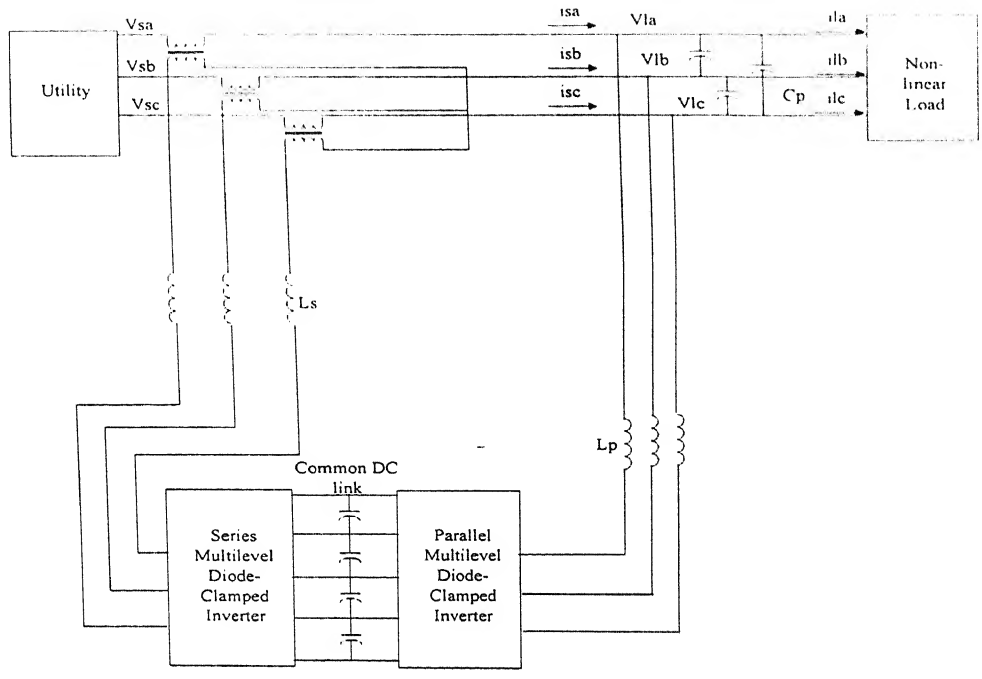

Fig. 2.18 Series–parallel connection to electrical system of back-to-back multilevel diode-clamped inverters for universal power conditioner.

2.4 Conclusion

A survey of various power circuit configurations and control strategies of Power Quality Conditioners has been carried out in this chapter. The important observations are summarized below.

- VSI has come up as a standard converter for active power filer applications.
- Due to fast acting controllers, time domain applications have been efficiently implemented.
- In DVR, it is found that quadrature injection does not require steady state active power, and this type of control is suitable for low power factor load.
- For very high power applications, three-level inverter has also been reported, but more than one capacitor in the common dc link inherently carries the problem of

voltage unbalance between the two capacitors and additional measures are to be taken to compensate that.

- Most applications have been reported for three phase four wire systems for UPQC.
- Single phase control schemes for UPQC are not investigated.
- Experimental investigations on UPQC control, simultaneously involving closed-loop series and shunt converter operation are inadequate.

Under these findings, it is important to note that UPQC is a potential custom power equipment, which requires extensive exploration and which may bring out promising capabilities. Therefore, attempts have been made to investigate the potential of UPQC, with a particular emphasis on UPQC with quadrature voltage injection (UPQC-Q). The present dissertation is primarily focused to design, simulate and experimentally implement both single phase and three phase UPQC under closed-loop control. Additionally, new control schemes are proposed, and some detailed simulation study are conducted to find suitable active power filters for high power applications.

Chapter 3

Single Phase Unified Power Quality Conditioner

3.1 Introduction

The development of a single phase power quality conditioner precedes the development of a three phase topology. A single phase power quality conditioner can be applied for low power applications supplying single phase critical loads. Additionally, the single phase topology can also be applied in rural electrification handling relatively small amount of power.

This chapter proposes a multipurpose power conditioning equipment, named Unified Power Quality Conditioner (UPQC), for a single phase system having the following facilities.

1. The Unified Power Quality Conditioner (UPQC) maintains load end voltage at the rated value in case of supply voltage sag.
2. It eliminates the harmonics in the supply current, thus improves utility current quality for nonlinear loads.
3. It provides the VAR requirement of the load, so that the supply voltage and current are always in phase, therefore, no additional power factor correction equipment is necessary.
4. The present scheme does not use any separate diode bridge rectifier or other energy storage device to support the dc link voltage for the series compensator, and does not inject any harmonics in supply current. The synchronous link converter maintains the common dc link voltage. Thus, in the situation where under-voltage is a severe problem, UPQC can maintain load end voltage at the desired level for indefinite period of time.

The injected voltage maintains quadrature advance relationship with the supply current, so no real power is consumed by the series compensator in steady state; hence the equipment is termed as **UPQC-Q** to highlight this aspect.

Unlike several existing Dynamic Voltage Restorer (DVR) schemes [40, 46], the voltage to be boosted in case of sag is always in quadrature advance to the supply voltage. Though quadrature injection of voltage requires additional capacity of series compensator, thus puts limitation on its range, this leads to a reduced VA rating of the shunt compensator as active power consumption by the series compensator is minimized. Additionally, the series compensator also shares a part of VAR of the load. A detailed loading analysis has been carried out to determine the rating of UPQC under different control strategies and the relative merit and de-merits are studied.

A new hybrid control scheme has been developed combining both the advantages of analog and digital controllers with the help of a PC for the experimental realization of a proposed system.

3.2 Power Circuit Configuration

The UPQC consists of two single-phase full bridge inverters connected in cascade as shown in the Fig. 3.1. Each limb of the inverter consists of two IGBT switches having anti-parallel diode across them. The inverter–II (Synchronous Link Converter VAR Compensator (SLCVC)) is connected in parallel to the load (which may be linear or non-linear) through a synchronous link inductor, L_{SLC}. The inverter–I (Series Compensator (SC)) is connected in series with the supply voltage through a low pass R-L-C filter and transformer. The SC operates in a PWM voltage controlled mode. It injects voltage in quadrature advance to the supply voltage (current) such that the load end voltage is always maintained at the desired value. Further, this ensures that the SC does not consume any active power.

The main objectives of the SLCVC are to compensate for the reactive power demanded by the load to eliminate the harmonics from the supply current and to regulate the common dc link voltage. The SLCVC operates with hysteresis current controlled mode to make the supply current in phase with the supply voltage.

The two inverters operate in a coordinated manner with a distinct hierarchy, which is elaborated in section 3.4.

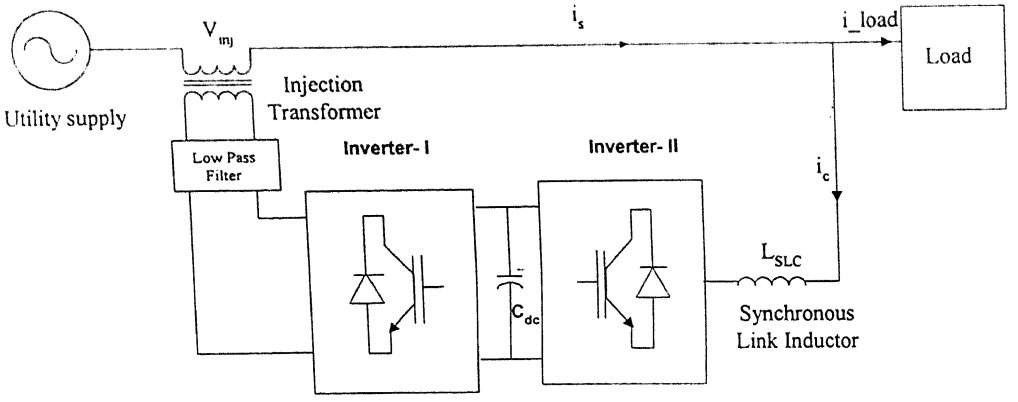

Fig. 3.1 Schematic diagram of single phase UPQC

3.3 Operating Principles

The SLCVC part has to be discussed first to explain the operation of UPQC. SLCVC is a boost type, current controlled VSI as shown in Fig. 3.2a [19]. The current drawn from utility is forced to trace a sinusoidal reference template i_s^* within a fixed hysteresis band. The width of the hysteresis window determines the harmonic spectra of the source current, and the switching frequency of the SLCVC.

The dc link voltage is kept constant at a suitable value throughout, and it should be always at least more than the peak of the supply voltage to draw leading current. Turning 'ON' switches S_3 and S_4 will increase the source current within the band (as the dc link voltage is additive to supply voltage, as seen in Fig. 3.2b). When the upper limit of the band is hit, the current has to be reduced, and then S_1 and S_2 will be turned on (dc link voltage opposes the supply voltage as seen in Fig. 3.2c).

In the present scheme, the reactive VA requirement of the load is not sensed. The magnitude of the in-phase component of the load current is determined indirectly.

Assuming the power loss of SLCVC to be zero, dc link capacitor voltage should remain constant if supply current, i_s, is equal to the active component of the load current. However, there are losses in the converter, which has to be replenished from the stored energy of the capacitor. This results in reduction in capacitor voltage. In order to maintain the capacitor voltage to its desired value, the losses of the converter have to be supplied from the utility itself. This is achieved by choosing a proper value of reference source current, i_s^*.

Now, with the increase of active or reactive component of load current, the capacitor voltage will vary, and i_s^* has to be adjusted accordingly. Therefore, the error of the dc link voltage is processed through a PI controller to generate the magnitude of i_s^*.

Since, the source current is bound within a narrow hysteresis band, lower order harmonics are eliminated. This is achieved without sensing or estimating the load current harmonics. The higher order harmonics (>>49) are eliminated by the source impedance.

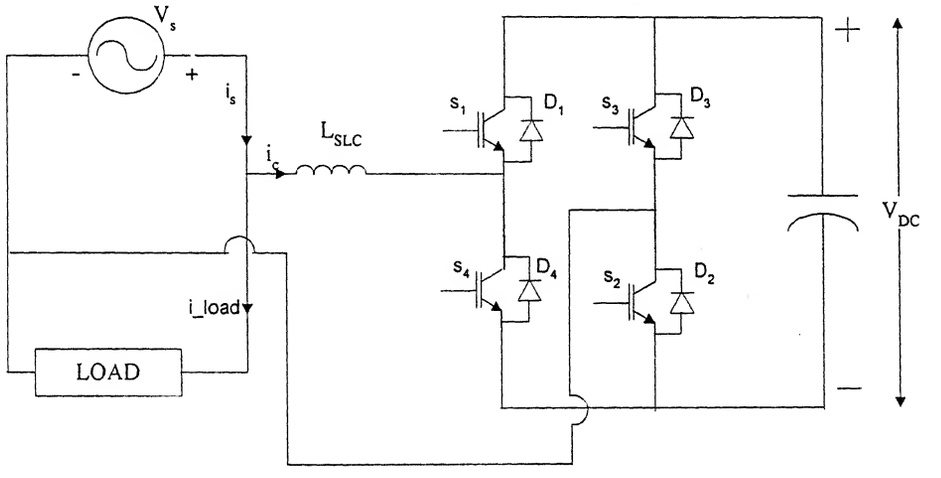

Fig.3.2a Schematic diagram of single phase SLCVC

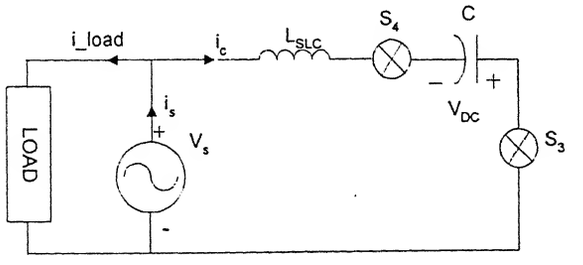

Fig.3.2b Current distribution diagram through SLCVC when switches S_3 and S_4 conduct

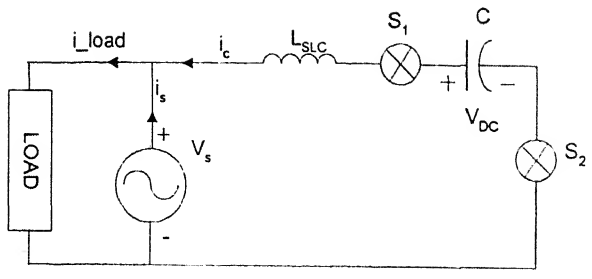

Fig.3.2c Current distribution diagram through SLCVC when switches S_1 and S_2 conduct

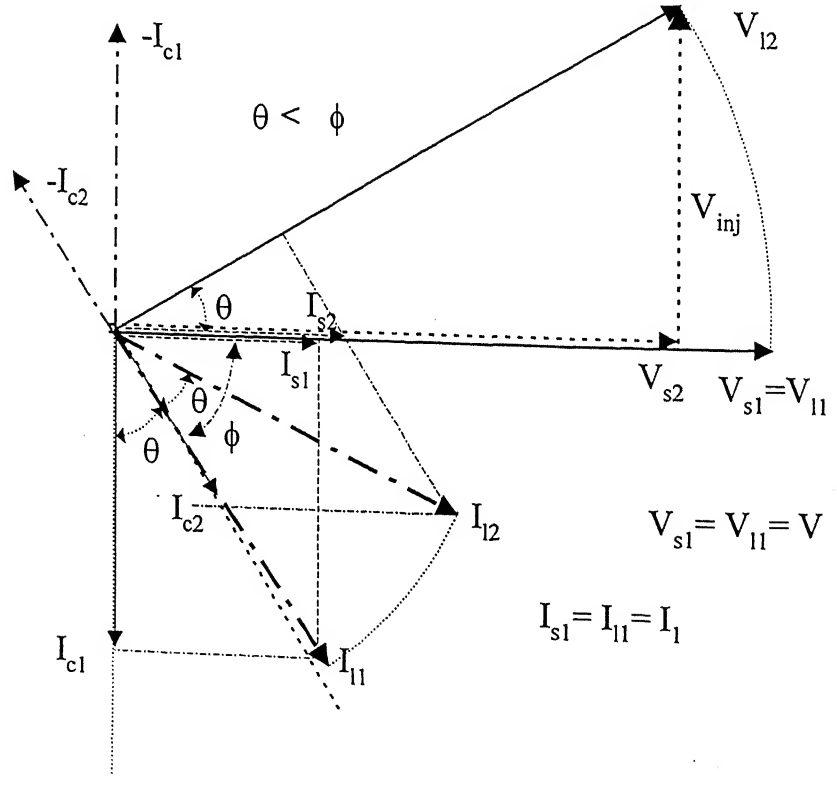

Fig. 3.3a Phasor diagram of UPQC-Q for fundamental power frequency, when $\theta < \Phi$

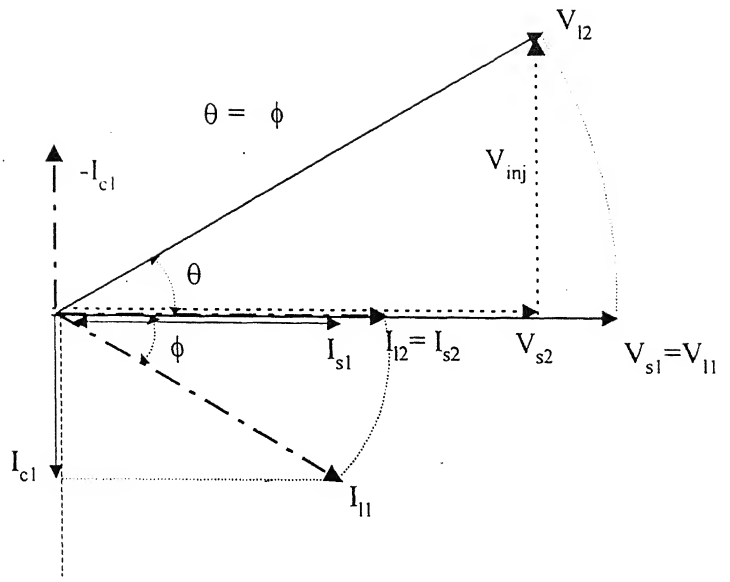

Fig. 3.3b Phasor diagram of UPQC-Q for fundamental power frequency when $\theta = \Phi$

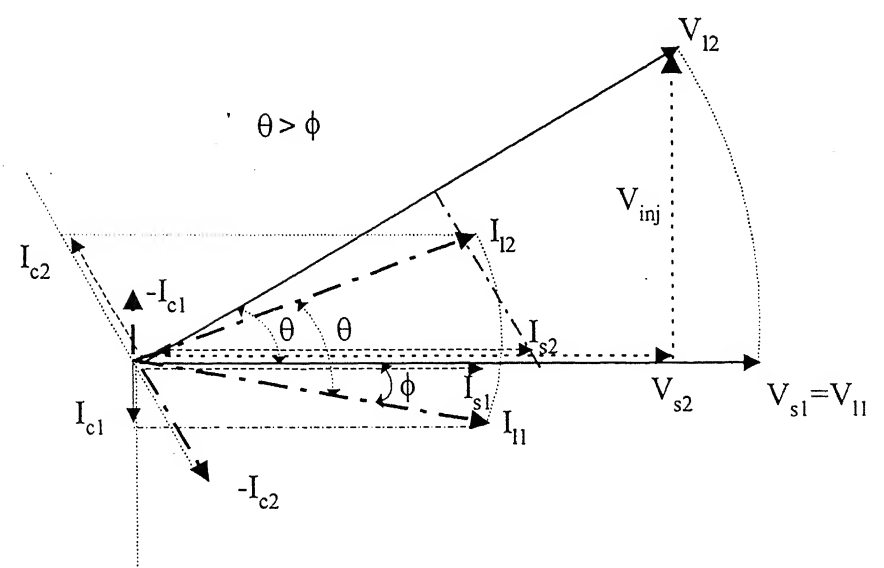

Fig. 3.3c Phasor diagram of UPQC-Q for fundamental power frequency when $\theta > \Phi$

Thus, $\mathbf{I}_{c2}$, as shown in Fig.3.3b, becomes zero. This is the minimum loading condition or zero VA loading of the shunt compensator. This will be further elaborated in the next section.

But, if the supply voltage sag is such that $\theta > \phi$ (Fig. 3.3c), then SLCVC current has to increase again to bring back leading power factor to unity. This condition may occur even with small voltage sag (say 15%) when load power factor is already high.

It is desired that I_{s2} should always be in phase with the supply voltage. Between the series and shunt converter control loops, the analog hysteresis current control loop for the shunt converter (SLCVC) is faster. For non-linear loads, harmonic elimination and VAR compensation are first done by the SLCVC, so the utility sees the load current to be always in phase with voltage and of desired sinusoidal shape. A slower digital controller simultaneously corrects the voltage sag. Due to faster compensation by the shunt controller, the series voltage compensator always sees the supply current to be in phase with the supply voltage. The two loop speeds are chosen such that in no case these two controllers can interfere with each other and cause instability. The details of the control scheme are provided in Section 3.5.

3.4 VA Requirement of UPQC-Q

The loading calculation has been carried out on the basis of linear load for fundamental frequency only. From Fig. 3.3 it can be found out that for each phase, the load voltage is to be kept constant at 1 p.u. irrespective of the supply voltage variation.

$$V_s = V_{l1} = V_{l2} = V_{s1} = Constant = 1\ p.u. \quad (3.6)$$

The load current is assumed to be constant at the rated value, i.e.,

$$I_l = I_{l1} = I_{l2} = 1\ p.u, \quad (3.7)$$

with fundamental p.f. = $\cos\phi$.

The active power demand in the load remains constant and is drawn from the source.

$$i.e.\ V_s I_s = V_l I_l \cos\phi = Constant \quad (3.8)$$

In case of a sag when $V_{s2} < V_{s1}$, where x denotes the p.u. sag,

$$V_{s2} = (1-x)\ V_{s1} = (1-x)\ p.u. \quad (3.9)$$

Now, to maintain constant active power under the voltage sag condition,

$$V_{s1} I_{s1} = V_{s2} I_{s2} \quad (3.10)$$

Or, $I_{s2} = (1.I_l \cos\phi)/(1-x) = \cos\phi/(1-x)$ p.u. (3.11)

As the voltage injected by the series inverter is in quadrature with the supply, the resultant load voltage V_{l2} makes an angle θ (Fig. 3.3) with the supply V_{s2}.

$$V_{inj} = \sqrt{(V_{s1}^2 - V_{s2}^2)}$$

$$\therefore \frac{V_{inj}}{V_{s2}} = \tan\theta,\ V_{inj} = V_{s2}\tan\theta\ ,\ V_{inj} = (1-x)\tan\theta \quad \text{p.u.} \quad (3.12)$$

$\therefore$ Series VA Rating = $V_{inj}.\ I_{s2} = \cos\phi\tan\theta$ p.u. (3.13)

The shunt inverter current can be calculated from the trigonometry of the vector diagram in Fig.3.3a.

$$I_{c2} = \sqrt{I_{l2}^2 + I_{s2}^2 - 2I_{l2}I_{s2}\cos(\phi-\theta)}$$

$$= \frac{\sqrt{(1-x)^2 + \cos^2\phi - 2\cos\phi\cos(\phi-\theta)(1-x)}}{(1-x)}\ p.u. \quad (3.14)$$

Therefore, the shunt inverter VA rating = $I_{c2}.V_{l2} + I_{c2}^2.Z_{SLC}$

$$= \frac{\sqrt{(1-x)^2 + \cos^2\phi - 2\cos\phi\cos(\phi-\theta)(1-x)}}{(1-x)} + \frac{(1-x)^2 + \cos^2\phi - 2\cos\phi\cos(\phi-\theta)(1-x)}{(1-x)^2} Z_{SLC}\ \ p.u. \quad (3.15)$$

Adding (3.13) and (3.15) the total VA rating of the UPQC-Q can be evaluated as

$$VA\text{-}Q = \cos\phi\tan\theta + \frac{\sqrt{(1-x)^2 + \cos^2\phi - 2\cos\phi\cos(\phi-\theta)(1-x)}}{(1-x)} + \frac{(1-x)^2 + \cos^2\phi - 2\cos\phi\cos(\phi-\theta)(1-x)}{(1-x)^2} Z_{SLC}\ \ p.u. \quad (3.16)$$

where Z_{SLC} is the p.u. impedenece of the synchronous link converter inductor.

Figs. 3.4 and 3.5 show the series and shunt VA loading of UPQC-Q respectively [62-63]. The six points in each set are for p.u. supply voltage sag from 5% to 30%. This range has been chosen as the most practical case as observed from survey reports [4]. A wide range of load power factor has been chosen from 0.25 – 0.9 lagging., The rating of the equipment can be estimated from (3.6- 3.16). In the present case, the series inverter rating will be 0.918 p.u (based on maximum loading at 30% sag at 0.9 lagging load p.f.).

As observed from the graph, it is seen that loading on the series inverter increases as % sag increases. The SLCVC rating will be 0.957 p.u. (based on maximum loading at 5% sag at 0.25 lagging load p.f to cater the mentioned region of voltage sag under the specified power factor.

SLCVC loading curve distinctly shows that loading on the inverter is mutually related with the load power factor and % voltage sag. For each power factor, certain percentage of sag creates the condition mentioned in (3.5), i.e. zero loading condition of the SLCVC. Thus there is a minimum loading locus for SLCVC, which satisfy the condition

$$x + cos\varphi = 1 \qquad (3.17)$$

As mentioned earlier if $\theta<\phi$, the two compensators shares the VAR of the load. But if $\theta>\phi$, then SLCVC current has to increase with the opposite sign to bring back leading power factor to unity, and this increases the loading of the SLCVC additionally.

It is observed that the individual converter maximum loading occurs at different power factor and sag condition, and Fig. 3.6 shows the combined VA loading of UPQC-Q. The combined rating of UPQC-Q will be summation of ratings of both inverters , i.e. 1.875 p.u.

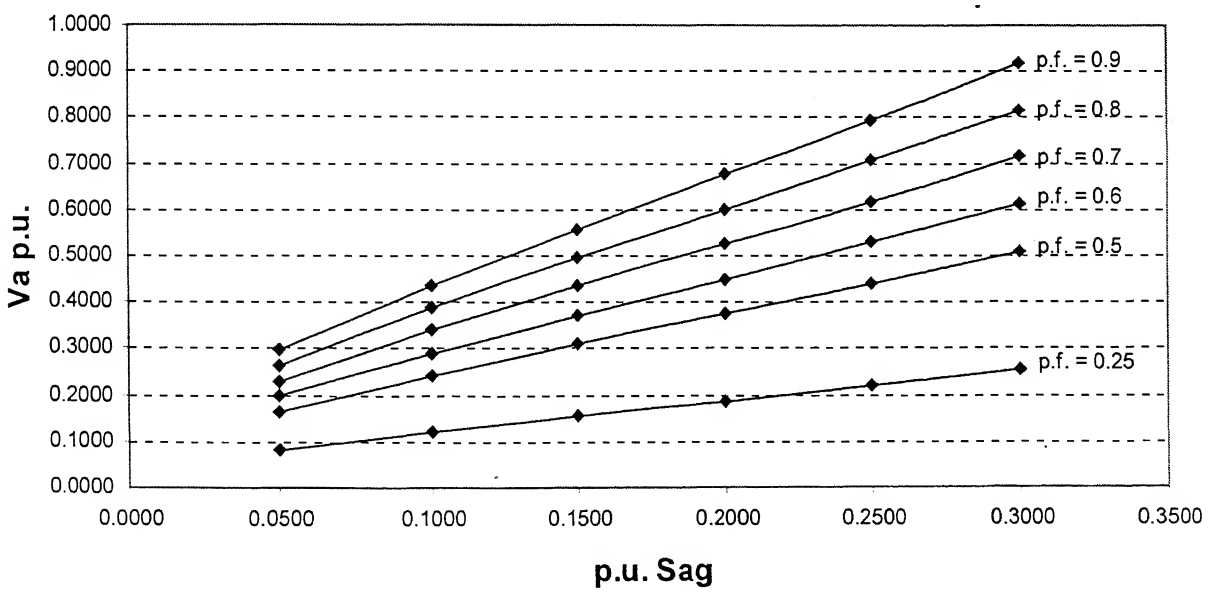

Fig.3.4 Series VA loading of UPQC-Q

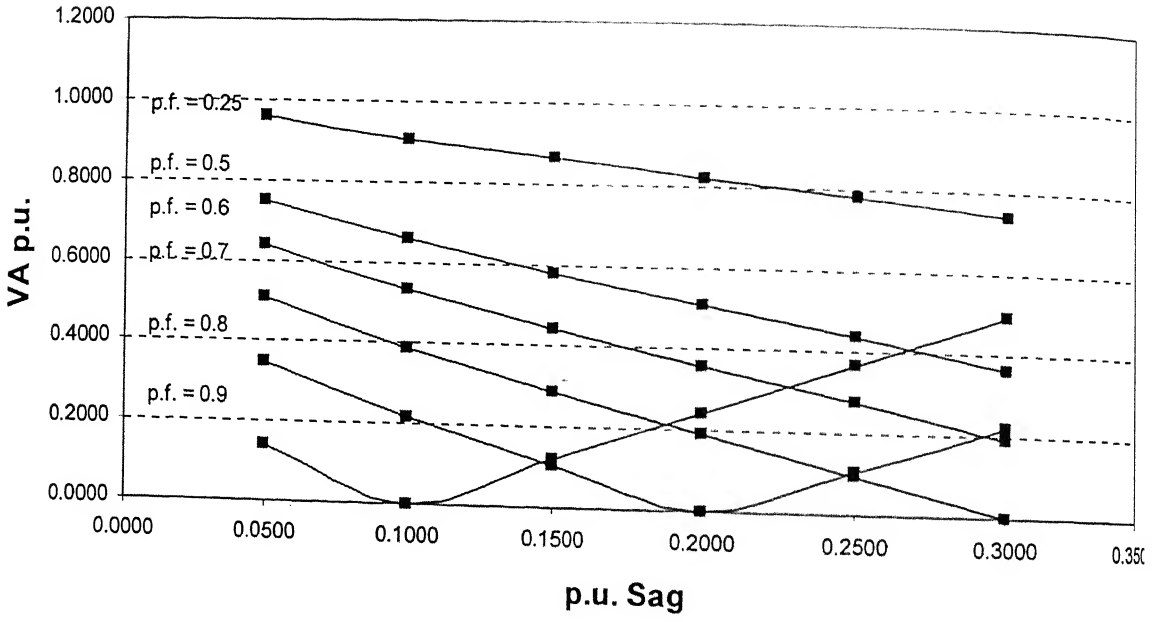

Fig.3.5 Shunt VA loading of UPQC-Q

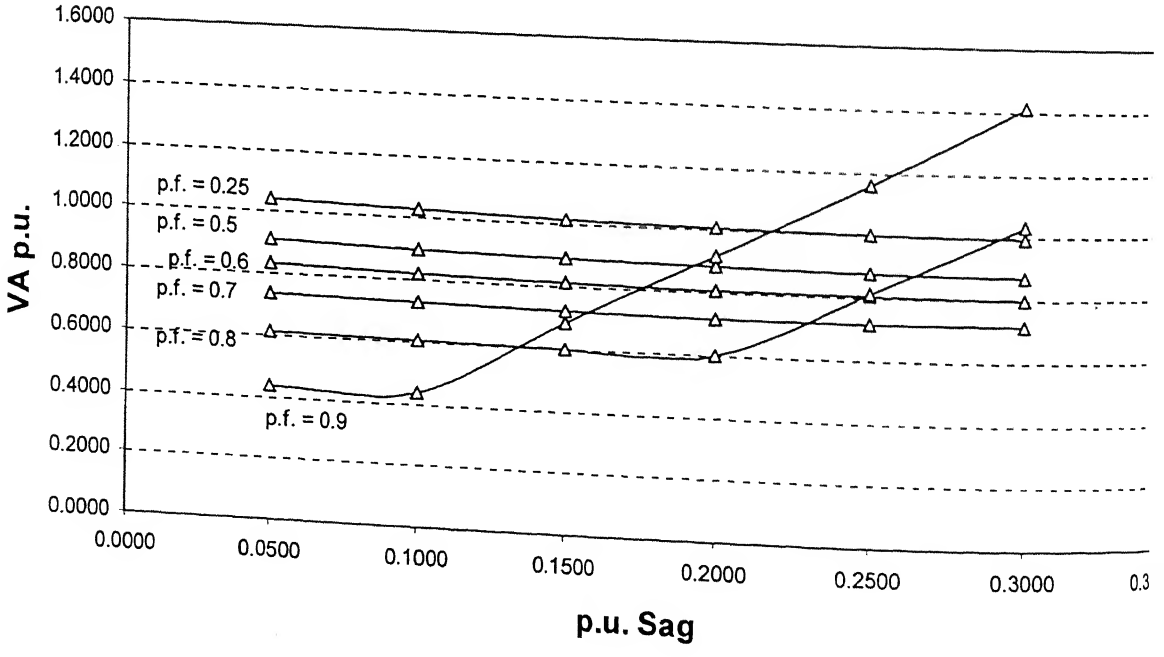

Fig.3.6 Combined loading of UPQC-Q

3.5 Control Strategy

To enhance the speed of response and also to retain the flexibility to modify parameters of the controller, a hybrid controller has been proposed with suitable analog and digital circuits. The control strategy consists of four modules.

Figure 3.7 shows the block diagram of the controller used for UPQC-Q.

a) ***Controller for DC Link Voltage:***

V_{dc}* (reference) is selected depending upon the maximum VAR to be compensated and the percentage sag (x%) to be mitigated. The error in the dc link voltage (V_{dc}* - V_{dc}) gives a direct measure of active power requirement of both load and UPQC from the supply.

Here the dc link voltage control is completely a PC based software control. After the dc link voltage (V_{dc}) is sensed through AD ch-0 and compared internally with the reference dc link voltage (V_{dc}^*), the error is passed through a software PI controller. As mentioned earlier, the error acts as a measure of the peak amplitude of reference supply current ($I_{ref(mag)}$), which takes care of the active current demand of the load and the charging current to maintain the dc link voltage to its reference.

b) ***Current Controller for SLCVC:***

$I_{ref(mag)}$ is multiplied by the sinusoidal template (in phase with the supply voltage) through an external DAC channel of PCL-208 to produce the reference current for the supply (i_s^*). A hysteresis band is selected around the reference current and the actual supply current (i_s) is confined within the hysteresis band. Whenever i_s hits the upper or lower limits of the band, switching takes place in the SLCVC so as to bring back the supply current within the band. There are three major factors associated with the switching frequency of the SLCVC, namely the window-width of the hysteresis band, the magnitude of the synchronous link inductor (L_{SLC}) and the differential voltage between the dc link and the ac supply. Wider window-width reduces the switching frequency of SLCVC but the harmonic content in supply current increases. If the magnitude of L_{SLC} increases, the rate of rise of current within the band reduces, consequently the switching frequency reduces, but on the contrary, that reduces the VAR compensating capability of the SLCVC and also slows down the dynamic response of SLCVC. Therefore, a trade-off has to be obtained in the design between the window-width, switching frequency and the value of the

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synchronous link inductor L_{SLC}. It is obvious that for better spectrum of the supply current, the hysteresis controller needs to be fast and accurate and it is implemented with analog control to circumvent the speed limitation of data acquisition cards.

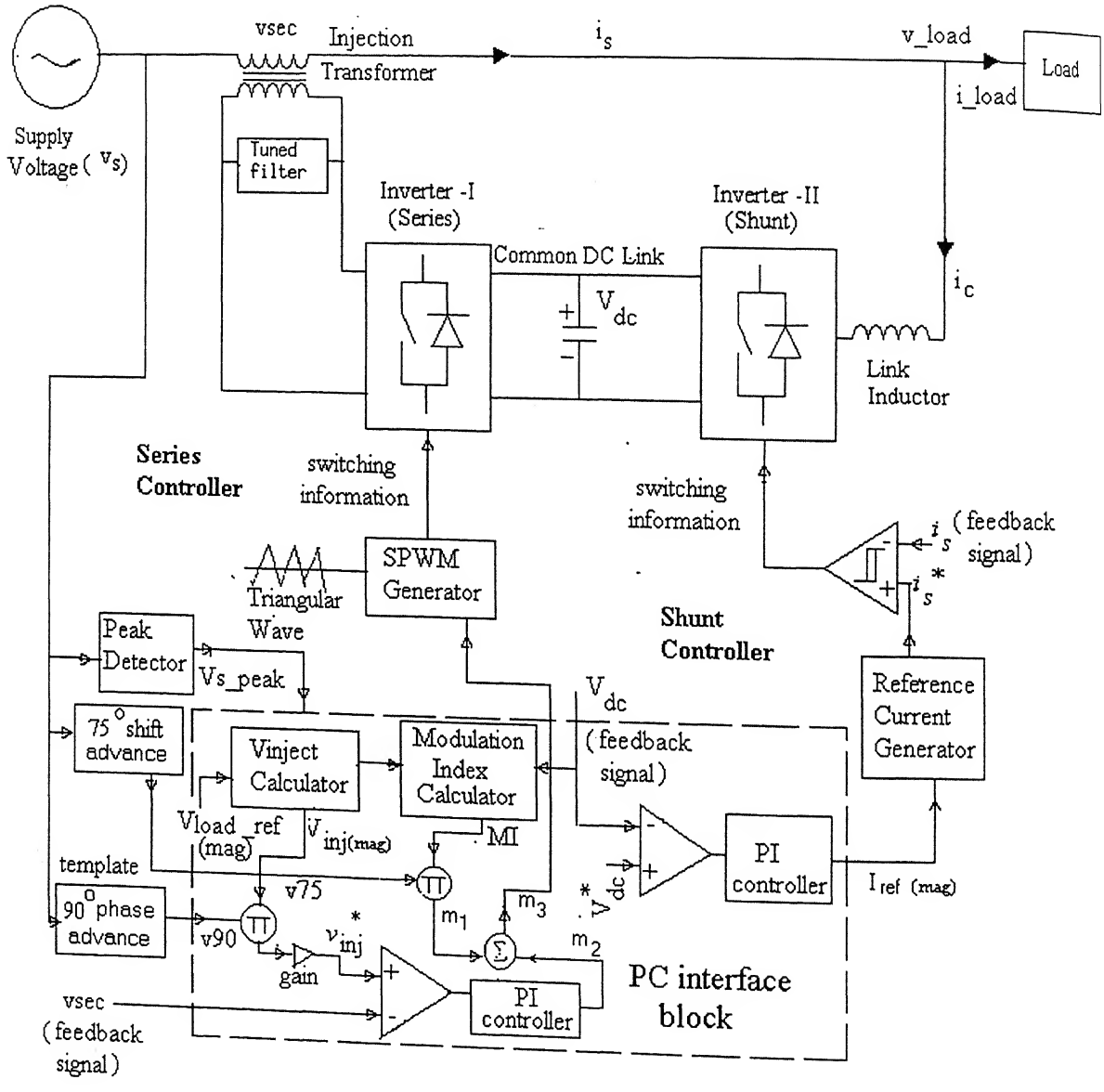

Fig. 3.7 Control block diagram of UPQC-Q

c) ***Dynamic Sag Controller:***

For the series compensator, the supply voltage peak (Vs_peak) is sensed through AD ch-1 and the 'Vinject Calculator' and the 'Modulation Index Calculator' find out the modulation index (MI) (Fig. 3.7). An appropriate sinusoidal template, which takes care of the phase shift due to the low pass filter at the output of the series compensator (75° shift advance (v75) in Fig. 3.7) is generated for the quadrature injection. It is sensed through AD ch-2, and after being multiplied by MI produces the nominal modulating signal m_1, of the feed-forward loop.

The actual voltage injected (*vsec*) is sensed through AD ch-4 and compared internally with the reference injected voltage (v_{inj}^*). v_{inj}^* is generated by multiplying a 90° phase advance sinusoidal template ((v90) sensed by AD ch-3) with the calculated magnitude of the injected voltage ($V_{inj\ (mag)}$). The injected voltage error is processed through a PI controller, which generates m_2. The control signal m_2 is added with m_1 to take corrective action on the modulating signal (m_1) for the series converter. Hence the PI controller is responsible to do the finer incremental adjustment of the modulating signal based on injected voltage error, which may occur due to load current variation. m_3 is the final modulating signal, which is compared with a triangular wave (5 kHz) to generate the switching signals for series compensator.

When a sag is detected such that $|V_{s2}| < |V_{s1}|$ (rated), $V_{inj} = \sqrt{(V_{s1}^2 - V_{s2}^2)}$

From PWM method [64],

$\sqrt{2}V_{inj} = MI\ (V_{dc}/2)$, where MI is the modulation index (MI). Therefore,

$$MI = (2\sqrt{2}\ .V_{inj})/V_{dc}. \qquad (3.18)$$

And if x is the p.u. sag to be mitigated, minimum dc link voltage is given by

$$V_{dc} = 2\sqrt{2}\ .\sqrt{x(2-x)}\ .V_{s1}, \qquad (3.19)$$

for maximum MI =1 (taking the transformer turns ratio to be 1:1).

d) *PWM Voltage Controller:*

Through sine-triangle comparison, fixed frequency PWM signals are generated and are sent to the drive circuit of the SC. The modulating signals are generated according to the amplitude of sag to be mitigated and the turns ratio of the injection transformer.

Thus the hybrid control method maintains the accuracy, speed and flexibility, combining the advantages of analog and digital controllers.

3.6. Simulation Study

The proposed control scheme has been verified by elaborate circuit simulation in the software SABER Simulator, which can simulate the system very near to the manner it is practically implemented. The control circuits can also be simulated with analog and digital components. For the simulation study, a harmonic free ac voltage source is assumed and the desired load voltage is set at 230 V (rms).

Non-linear load is modeled as a diode bridge rectifier with a series R-L Load of value (R = 5 Ω, L = 9 mH on dc side). The value of synchronous link inductor is 18 mH. The LPF values are: L = 7 mH, C = 60 μF. The hysteresis band has been taken as 0.09 A in the control circuit.

Fig. 3.8 shows the dynamic performance of UPQC under a supply voltage sag of 20% (i.e. supply voltage falls to 184 V). At the instant of occurrence of voltage sag, load voltage is seen to have a momentary dip of 15%, but within next cycle it retrieves to its rated value. After 5.5 cycle of sag condition when the supply voltage is restored to its original value, the load voltage undergoes a transient overshoot of 20%, but it comes back to the rated value within the next cycle. The above mentioned overshoot and undershoot are dependent upon the instant of occurrence of sag, and associated control delay.

Fig. 3.9 shows that even under fluctuating supply voltage condition, the supply current is sinusoidal and in phase with the supply voltage. It is also observed that to meet the active power requirement of the load, the supply current increases as the supply voltage falls.

Fig. 3.10 shows the harmonic analysis of the load voltage when it is maintained at 230 V, and the supply voltage is at 184 V. The THD of the load voltage is found to be merely 2%.

Fig. 3.11 shows the supply voltage and load current profile. The diode bridge rectifier load has displacement factor very near to unity. When a supply voltage sag occurs for a high p.f. load and UPQC injects a leading voltage to maintain the load voltage, the displacement factor of the SLCVC current with respect to the supply voltage changes from leading to lagging (as mentioned in section 3.3). The corresponding result is presented in

Fig. 3.12 for the condition described in Fig. 3.3c. As shown, the phase angle of the SLCVC current shifts, when the voltage sag is being compensated.

The performance of UPQC-Q under dynamic change in load condition is also presented in Fig. 3.13. When the load current is increased from around 8.5 kVA (load current 37.5 A) to 12 kVA (load current 52.46 A), the supply current also increases. At all instants the supply current has been found to be sinusoidal and the input power factor is unity. The Fourier analysis of load current and supply current has been presented in Fig. 3.14. It is seen that the load current THD is 10.63% (with 3rd, 5th and 7th harmonic contents are 8.2%, 4.9% and 3.26% of fundamental respectively). The supply current THD is observed to be 1.6% (below 5%, as specified by IEEE 519).

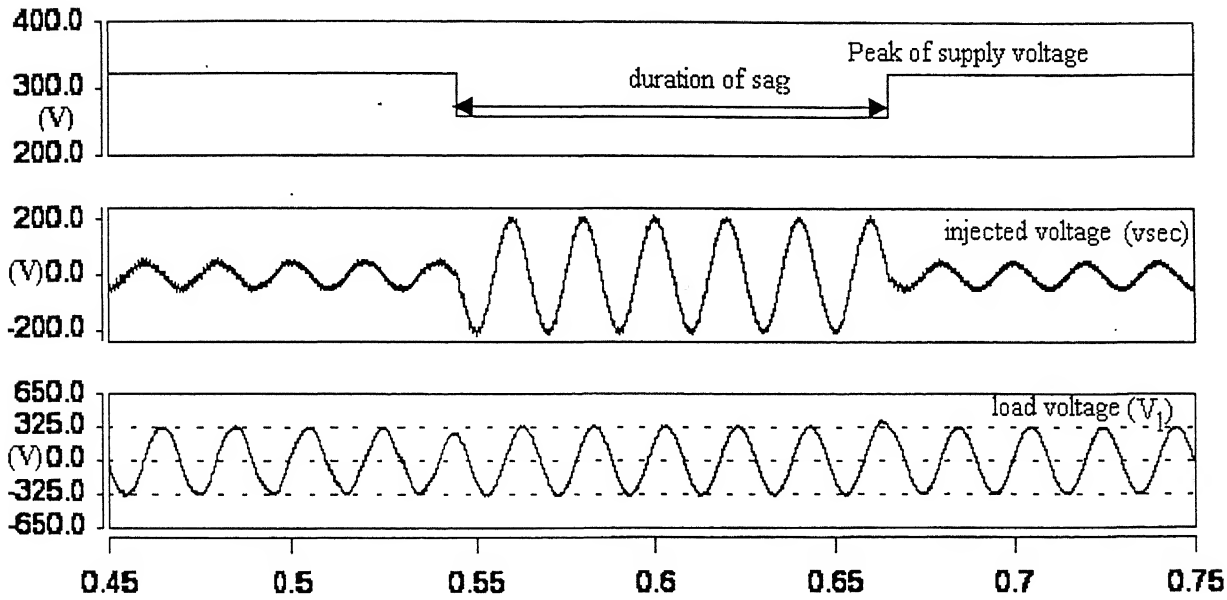

Fig. 3.8 Simulated result of load voltage, injected voltage under rated and 20% supply voltage sag condition

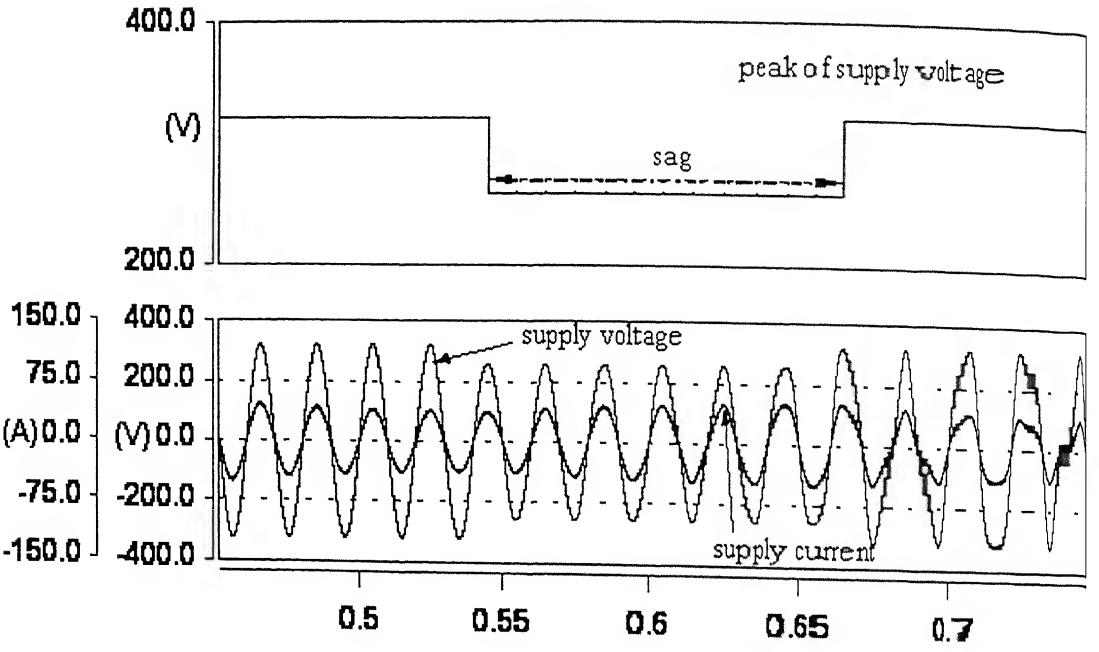

Fig. 3.9 Simulated result of supply voltage and current under rated and 20% supply voltage sag condition

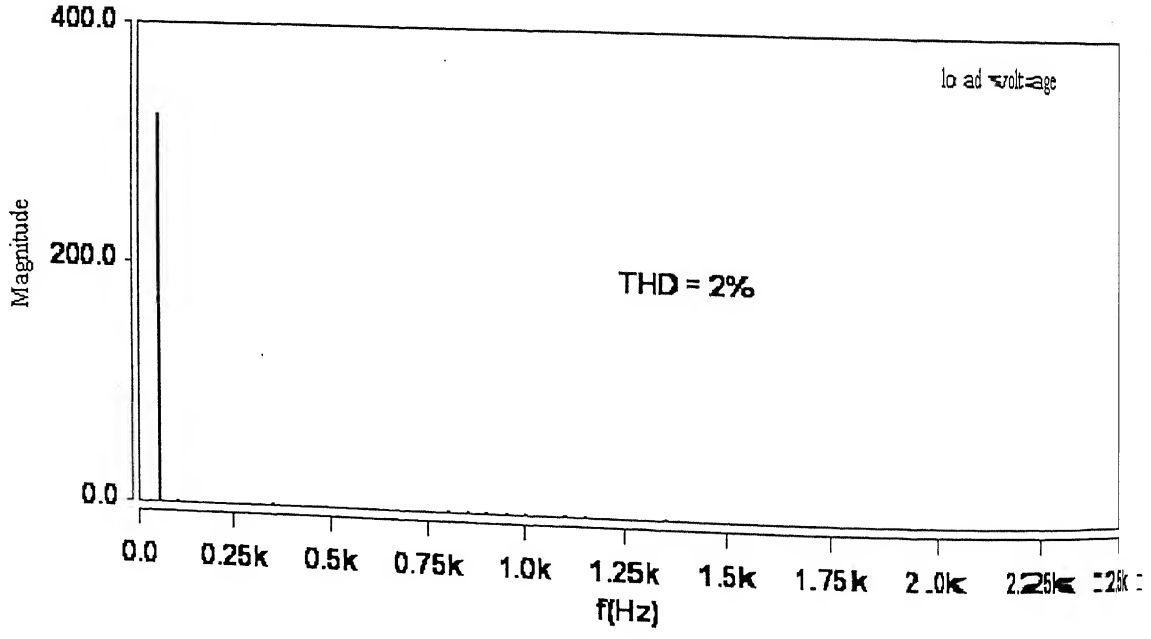

Fig. 3.10 Load voltage spectra

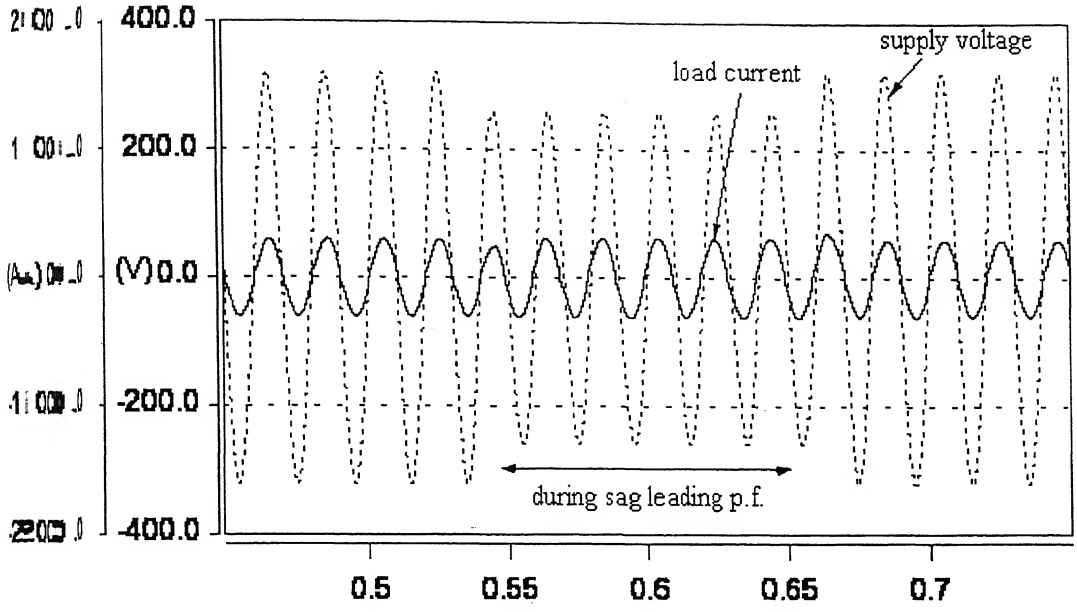

Fig. 3.11 Supply voltage and load current under normal and 20% supply voltage sag condition

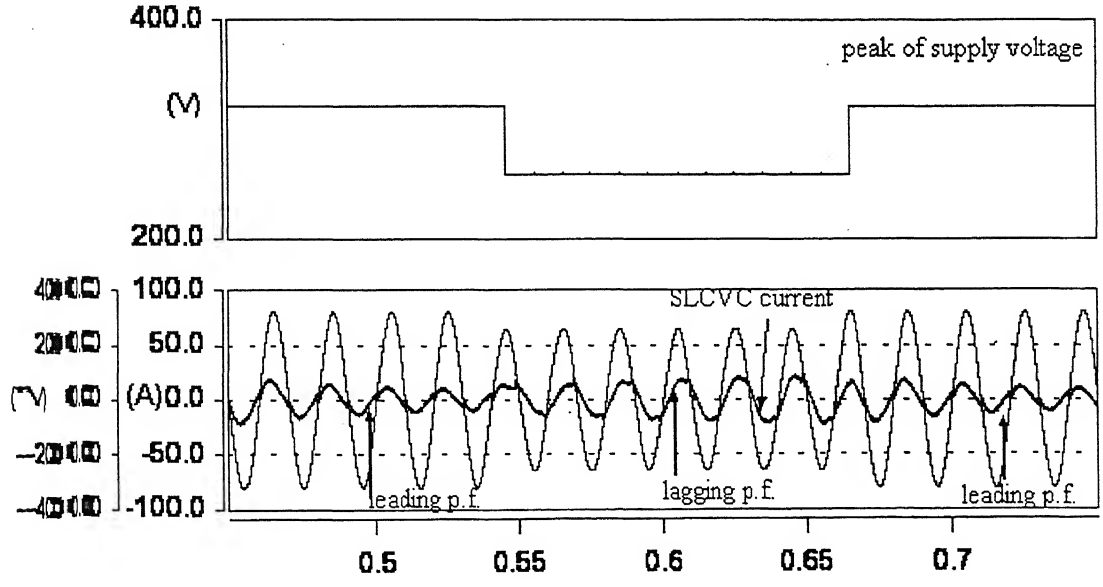

Fig. 3.12 Supply voltage and SLCVC current under rated and 20% supply voltage sag condition

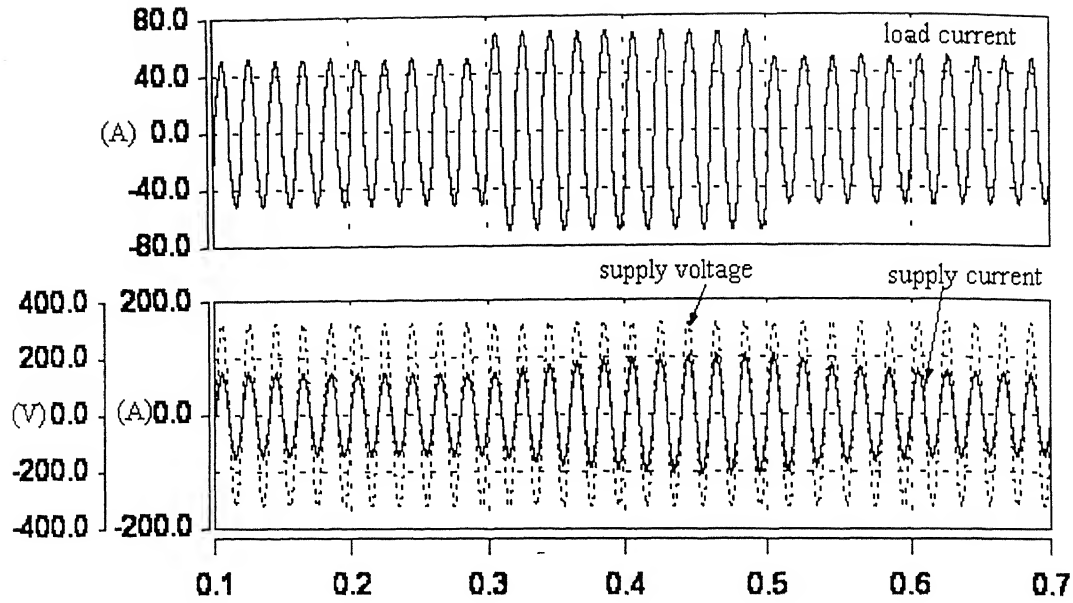

Fig. 3.13 Dynamic load current change and supply voltage and current

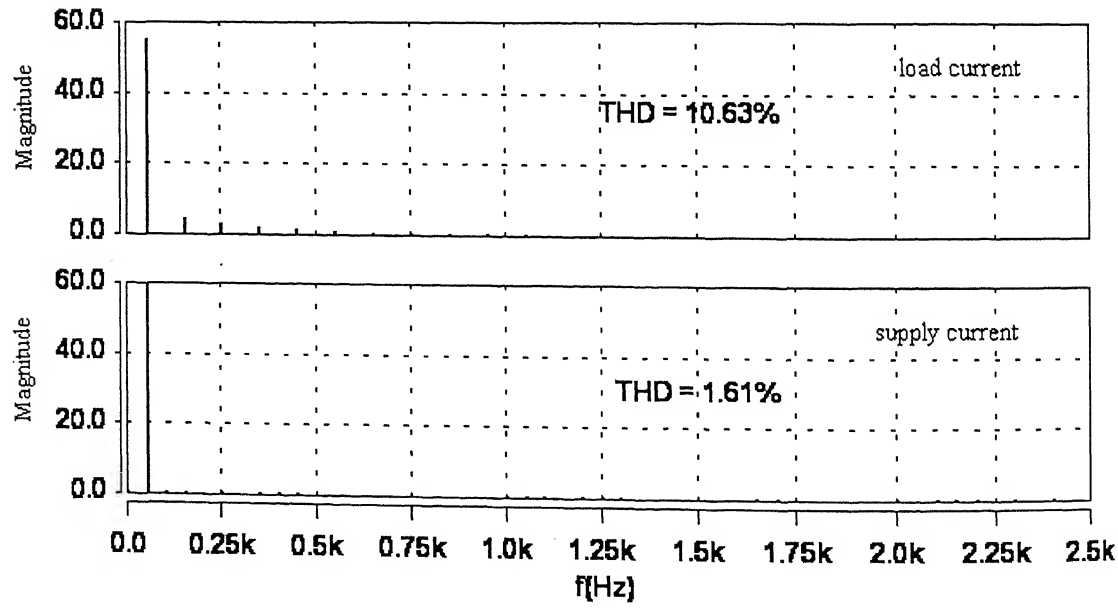

Fig. 3.14 Load current and supply current spectra

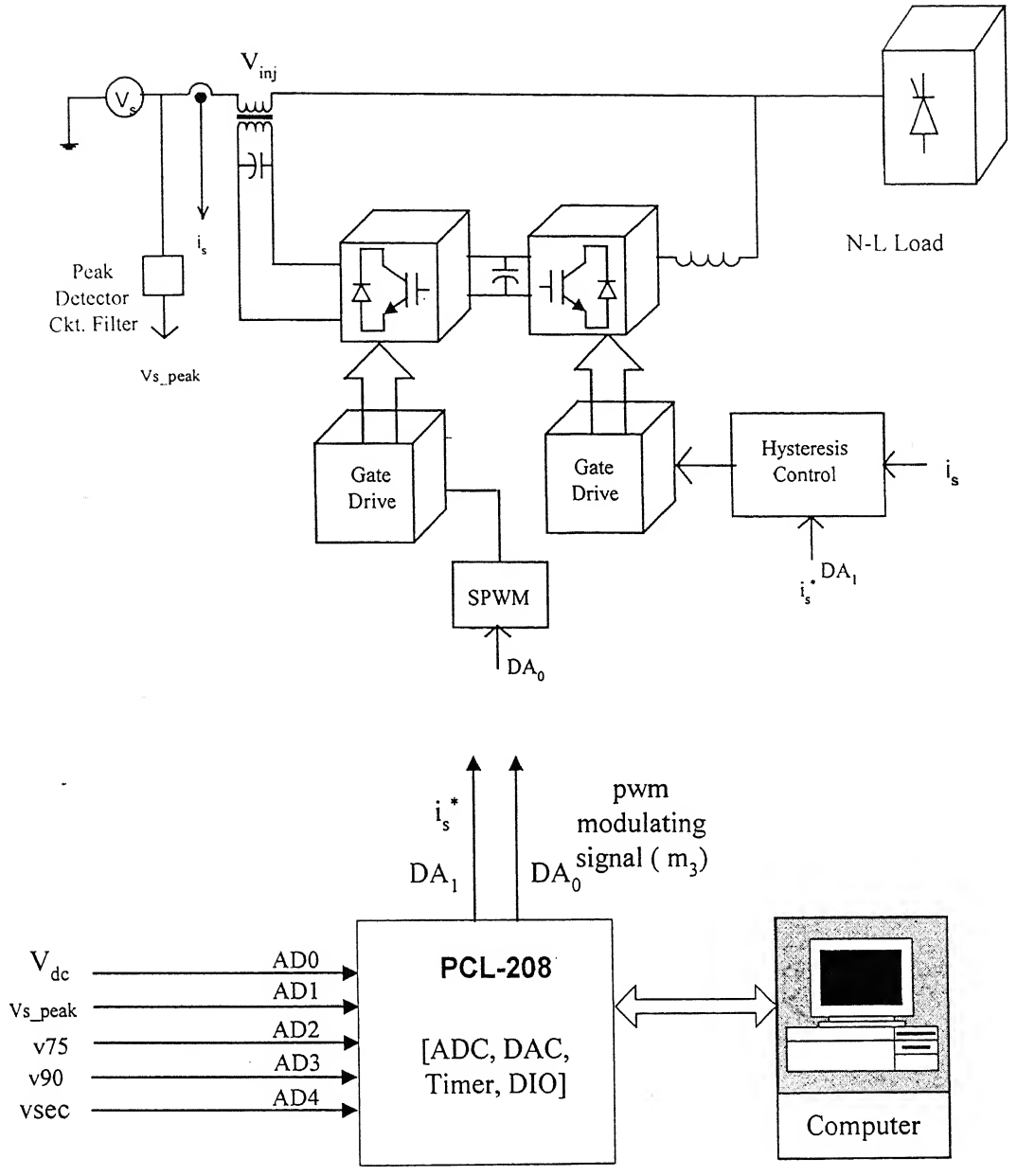

Fig.3.15 Block diagram of hardware implementation

3.7. Experimental Setup and Implementation of Control Circuit

After extensive simulation of the proposed system, a laboratory prototype UPQC set-up for experimentation has been designed and fabricated. Some of the components have been chosen according to the availability, and the aim has been to **qualitatively** verify the proposed control philosophy. The design details of the control circuitry are discussed. The experimental results obtained in steady state and dynamic conditions have been reported in the subsequent sections.

The control circuit is hybrid in nature, partly implemented with analog circuits and partly with digital ones using a Pentium –II 333 MHz, PCL-208 data acquisition card. This implementation helps in achieving smaller sampling time. Fig. 3.15 shows the schematic block diagram of the experimental setup. Analog and digital circuits are built in modular cards. Working aspects of a few typical control blocks and their actual circuit implementation are discussed in the following sections.

3.7.1 Implementation of the analog current controller

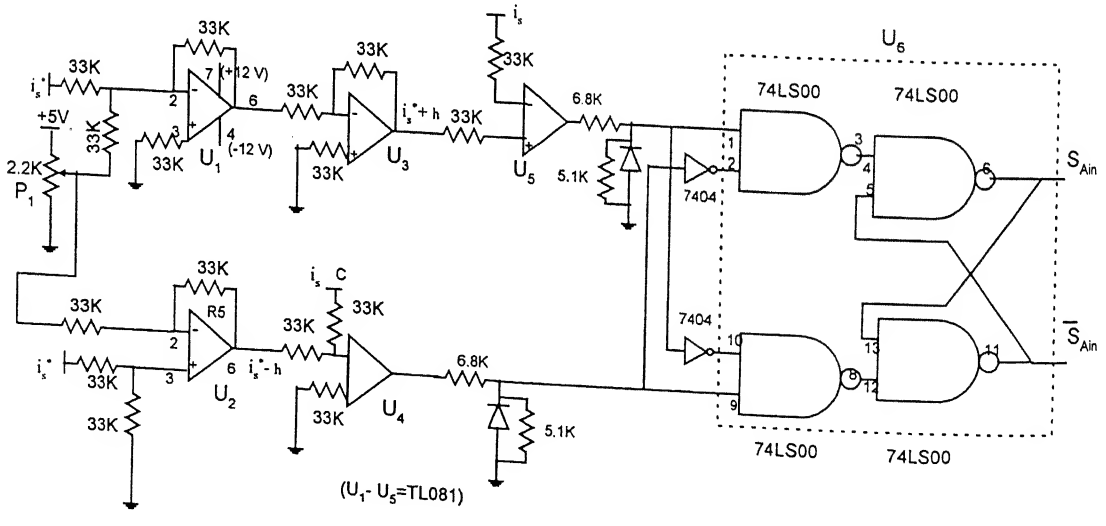

Fig. 3.16 Hysteresis current controller for SLCVC switching

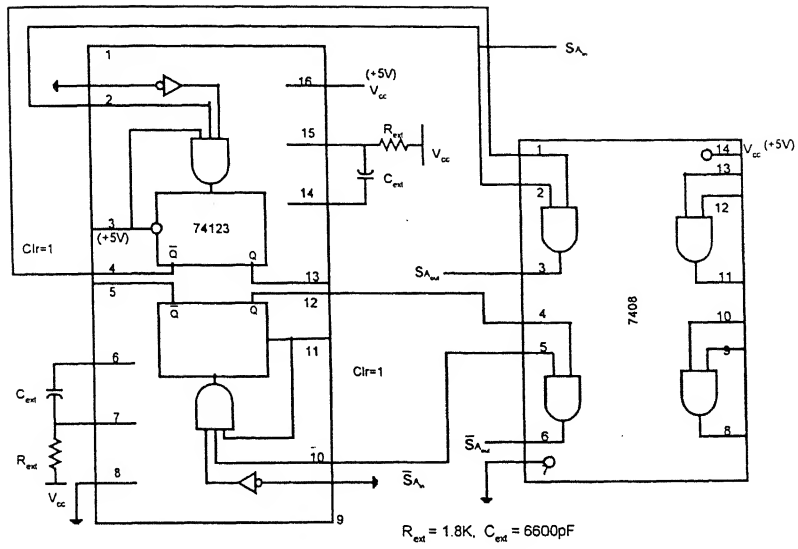

Fig. 3.17 Lock-out circuit

The hysteresis current controller, which keeps the supply current sinusoidal within a band, is shown in Fig.3.16. Op-amps U1, U2 and U3 establish the hysteresis window (i_s^* ± h) around the reference current i_s^*. The window height is controlled by the potentiometer P_1. U4 and U5 compare the source current i_s with the upper and lower bands [65]. U6 (7400) latches the outputs S_{Ain} and $\overline{S}_{Ain}$ to provide the steady switching status to S_1, S_2 and S_3, S_4 (Fig. 3.2a). During the rise of i_s, S_3, S_4 conduct. The other pair conducts during fall of supply current. Lock-out delay circuit provides delay (Fig. 3.17) between S_{Ain} and $\overline{S}_{Ain}$ to avoid the shoot-through fault due to simultaneous turn on of both the upper and lower switches in the same limb. Selection of proper values of R (1.8 kΩ) and C (6600 pF) in retriggerable monostable chip 74123 controls the delay. With the chosen value, the observed delay is 5 μs. The actual signals which go to trigger the switches are S_{Aout} and $\overline{S}_{Aout}$.

3.7.2 Implementation of DC link voltage control

A part of the controller is realized by software. The blocks inside the dashed rectangle in Fig. 3.7 shows the PC-based software implementation. After sensing and averaging the dc capacitor voltage, the signal is sent to PC through ch- 0 of ADC of PCL-208 [67] (Fig. 3.15). The voltage and current sensor details are given in Appendix-A. Inside the PC, the signal is compared with the reference dc link voltage value and the error is processed through the PI controller to generate the magnitude of reference current. The reference current magnitude is multiplied with a sinusoidal template and is available to the external analog circuitry through DAC ch-1 (DA_1) of PCL-208. The signal is filtered from noise and is multiplied with proper gain. The resultant signal acts as i_s^* and is sent to the hysteresis current controller circuit.

3.7.3 Implementation of dynamic sag controller

The supply voltage is stepped down and full-wave rectified. The rectified voltage is sampled with sample and hold (S/H) chip LF 398 at peak of the supply voltage as shown in Fig. 3.18. The output of the S/H circuit, Vs_peak, is filtered and is sensed through AD ch-1. Inside the PC, the signal is compared with the pre-decided Vl_peak and the error is processed through a 'Vinject Calculator' (as mentioned in Sec. 3.5) to determine the peak of the amplitude of the voltage $V_{inj(mag)}$ to be injected by the SC. Two more sinusoidal templates, which are 90° (v90) and 75° (v75) ahead of the supply voltage respectively, are sensed through ADC ch- 2 and 3. The basis of selecting v75 has been explained in Appendix-B. $V_{inj(mag)}$ is processed through a Modulation Index calculator (as mentioned in Sec. 3.5) and the output is multiplied with v75 to generate the feed-forward loop (m_1) of the modulating signal m_3 in Fig. 3.15. The $V_{inj(mag)}$ is multiplied with v90 to generate the reference (v_{inj}^*) signal. The actual voltage injected (vsec) is sensed through AD ch-4, which is compared with v_{inj}^* and the error is processed through a PI controller inside PC. The output of the controller (m_2) (Fig. 3.7) is added with the feed-forward signal, to generate the final modulating signal, which is sent out through DAC ch-0 (DA_0), to the analog SPWM generator.

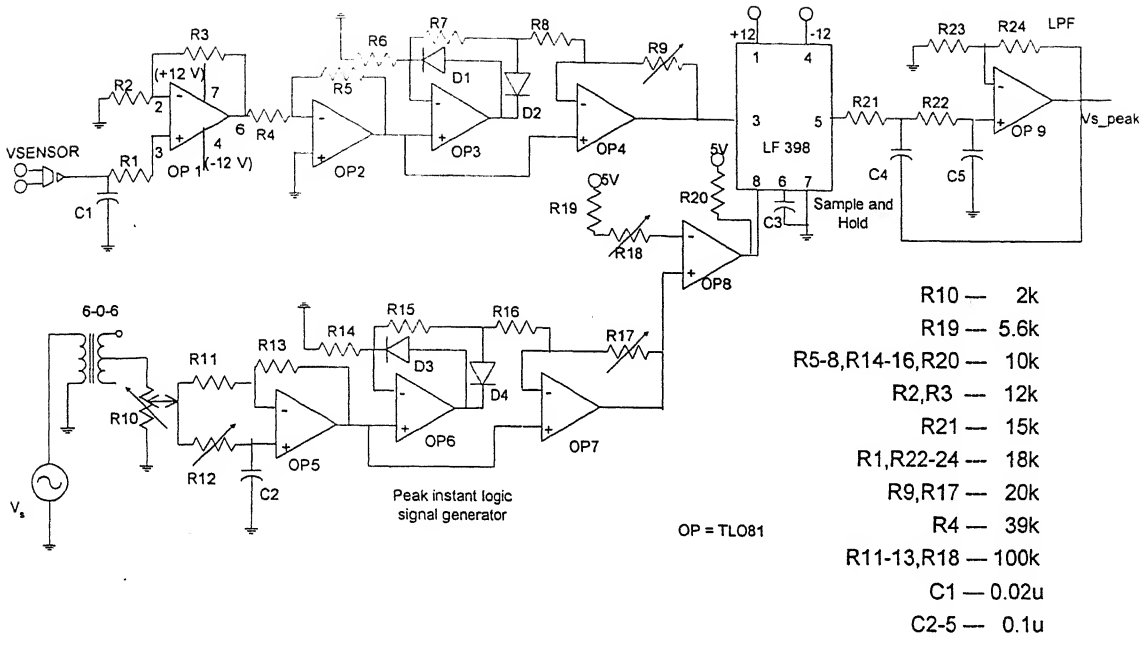

Fig. 3.18 Supply voltage peak detection circuit for sag detection

3.7.4 Implementation of series PWM voltage control

Fig. 3.19 shows the PWM generator circuit. DAC output is filtered and then compared with triangular wave of 5 kHz. The output is processed through a lock-out delay circuit. To enable or disable the control signals, a digital signal ***enbl*** has been used from PCL-208. If enbl=1, the circuit output signals (C_1 and C_2) are available with actual status at S_1, $\overline{S_1}$ and if enbl=0, S_1 and $\overline{S_1}$ are both zero. Fig. 3.20 shows how the signal m_3 is filtered and the dc bias is eliminated (which was due to unipolar DAC output). The signal is then properly scaled up to be fed into the PWM generator circuit as modulating signal B.

The gate driver circuit details have been given in Appendix-C.

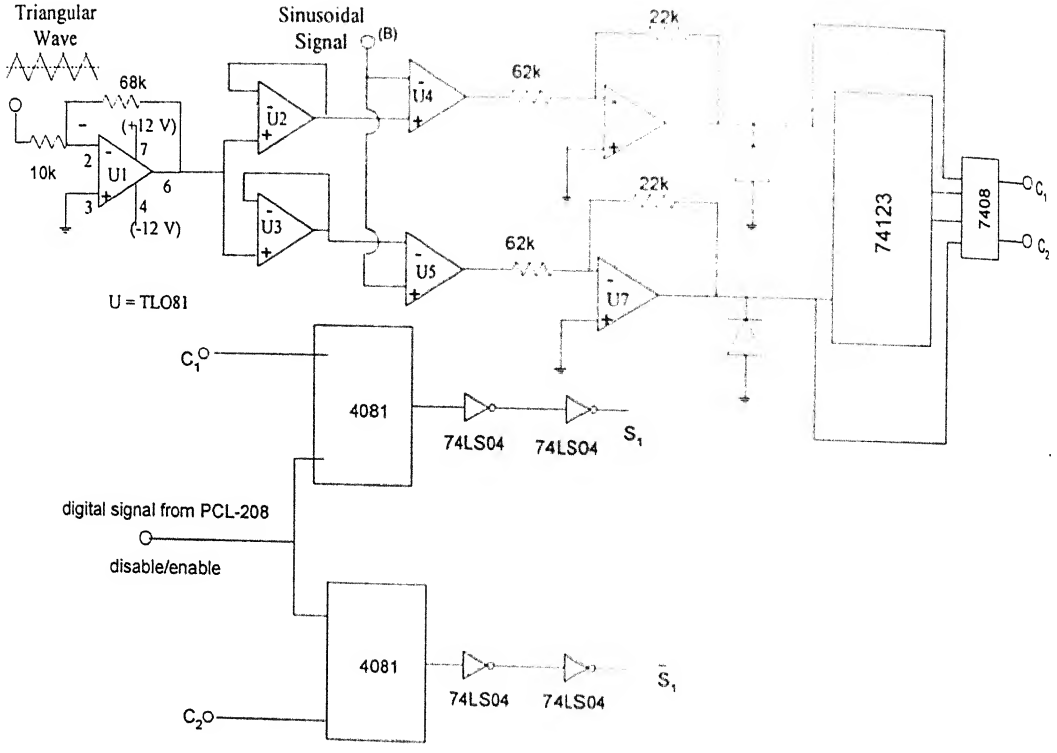

Fig. 3.19 Sin-PWM control for series inverter

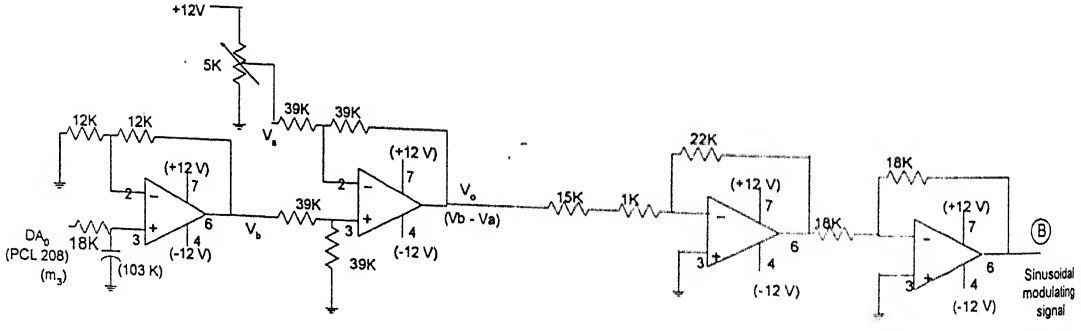

Fig. 3.20 Generation/processing of modulating signal for series inverter after DAC

3.7.5 Implementation of power circuit

A single phase prototype laboratory model of UPQC is fabricated to implement the proposed control strategy. The power circuit consists of the following main components.

- Two single phase IGBT based inverters, (IGBT switch, rating 50 A, 1200 V, make Fuji Electric (Japan), model 2MB150N-120. The IGBT switches and all diodes are mounted on suitable heat sinks to ensure proper heat dissipation. The IGBTs are protected with RCD snubber circuits of values R = 18 Ω, C = 0.01 μF, diode is MSBY239.

- One cascading electrolytic capacitor, Alcon make, rated 2200 μF, 400V DC.
- One diode bridge rectifier, using FSPR 25 P devices, for non-linear load. A 50 Ω, 5A, variable rheostat and 30 mH air core inductor are connected in series in the dc side of the rectifier.
- One iron core inductor (as synchronous link inductor) of 4.5 mH, 0.6 Ω.
- One injection transformer to connect the SC with the utility (rating 220 V:110 V, 1 kVA)
- One low pass filter has been used to eliminate the higher order harmonics of the PWM voltage of the Series Compensator. L = 4.3 mH, C= 60 μF, and the transformer magnetizing inductance = 200 mH.

3.8 Experimental Results

In this section, some typical experimental results are presented. Some of these results have been reported in [68]. The system parameters are given in Table 3.1. The PI controller gains of the dc link voltage control loop are $k_p = 0.3$ and $k_i = 0.6$, which have been found out by trial and error method. The trial was based on the performance of dc link voltage reaching its reference value and minimal transient oscillations respectively. In the dynamic sag controller the feed forward gain and the feed-back PI gains are $k_p = 0.02$, $k_i = 0.04$, which are chosen on a trial basis for fast response, dynamic phase shifting performance and minimum oscillation of sag controller.

The algorithm for coordinated control of UPQC is implemented in Turbo-C language; the computation of each cycle takes about 106 μsec. The speed is found sufficient for successful operation.

Table 3.1 System Parameters

System Voltage	54 V rms
Synch. Link Inductor	4.3 mH, 0.6 Ω
DC Link Capacitor	2200 μF,400V dc
Load Current Non-linear	1.8 A - 2.5 A
LPF parameter R= 0.6 Ω L= 4.2 mH C= 60 μF	
Transformer parameters Lp = 5.66 H Rp = 0.7 Ω Ls = 1.38 H Rs = 0.5 Ω	

3.8.1 Steady state performance

The steady state load current, source current, load voltage and source voltages are presented in this section.

For single phase non-linear diode bridge rectifier load, the load current nature is seen in trace 2 of Fig. 3.21, and its harmonics content is found to be 14.6% corresponding simulated result is given in Fig. 3.22. Fig. 3.23 shows the harmonic distribution in the load current. It is found that 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonics are 11.3%, 10.58%, 6.8% and 5.8% with respect to fundamental from the power scope measurement.

It can be observed that with the help of UPQC, the supply current remains sinusoidal in spite of the load current harmonics, as seen in the trace 1 of Fig. 3.21. Power scope measurement in Figs. 3.23 and 3.24 reveals the harmonic content in the load and supply currents. It is found that the measured supply current THD is only 3.75%, which is well within the permissible limit of specification (5%) of IEEE Standard 519. The 3^{rd}, 5^{th}, 7^{th} and 9^{th} harmonics have been reduced to 2.8%, 2%, 1.2% and .23% respectively. Similar conditions of Fig. 3.21 have been simulated in SABER and Fig. 3.22 satisfactorily matches the experimental results.

Fig. 3.25 shows the reference source current and the actual source current. Corresponding simulation result is shown in Fig. 3.26. The actual current follows the reference current within an appropriate hysteresis band.

Fig. 3.27 shows the phase relationship among voltages at different points of the system. Trace 1 shows the load voltage which has been maintained at 54 V, trace 2 shows the supply voltage. The supply voltage is reduced to 47.6 V. (This 11.8% sag has been created by suddenly loading the supply with an R load, which draws considerable current). The injected voltage is 26 V, which is injected in quadrature advance with the supply voltage, as observed in trace 3. The multiplication factor in trace 3 is 38. Comparable simulation results have been presented in Fig. 3.28. Fig. 3.29 shows the harmonic analysis of load voltage. The load voltage THD is found to be 3.6% from power scope measurement. The 3^{rd} and 5^{th} harmonics are 1.9% and 2.75% (individual harmonic<3% as specified by IEEE-519) with respect to fundamental. Fig. 3.30 and 3.31 show the experimental and simulated graphs of dc link voltage along with utility and load currents.

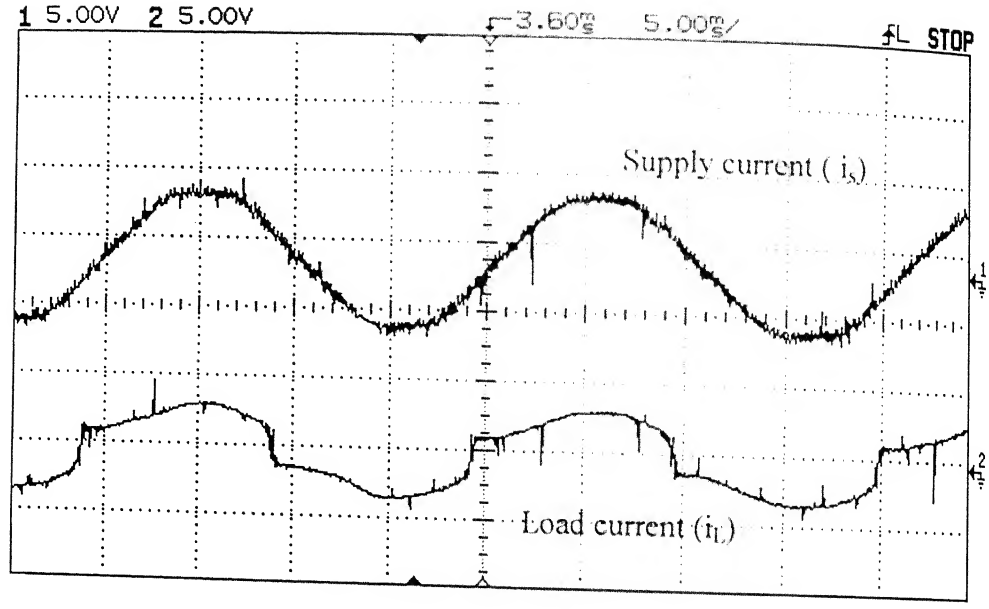

Fig. 3.21 Experimental result of supply current and load current
X axis : 5 ms/div Y axis: 5 A/div

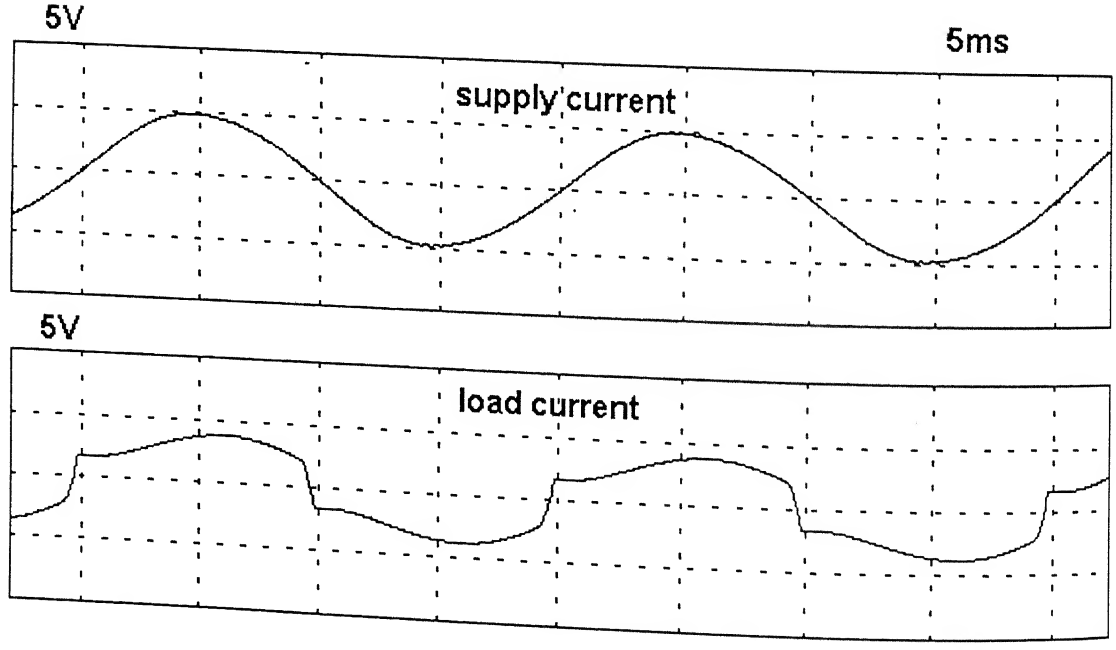

Fig. 3.22 Simulation result of supply and load current corresponding to Fig. 3.21
X axis = 5 ms/div Y axis = 5 A/div

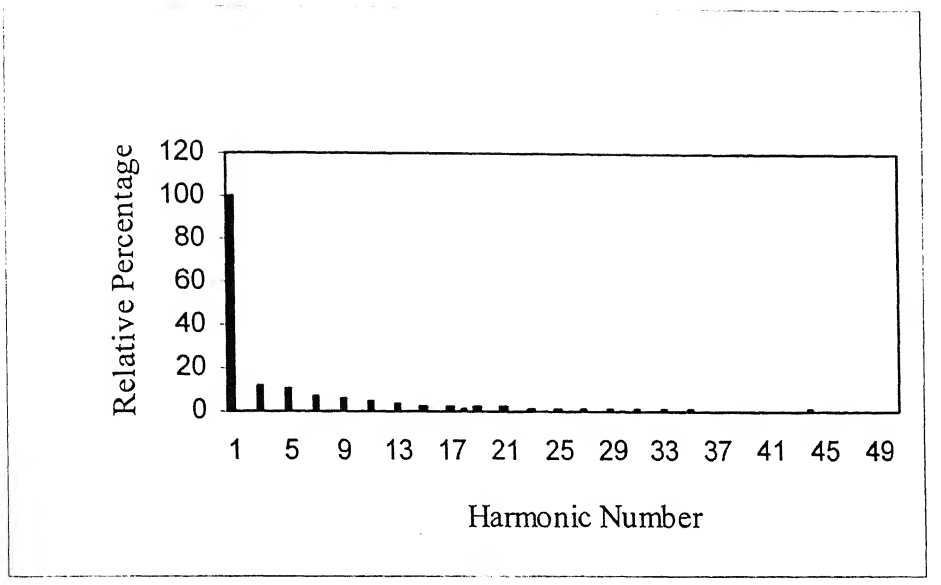

Fig. 3.23 Load current (i_load) spectra (Experimental)

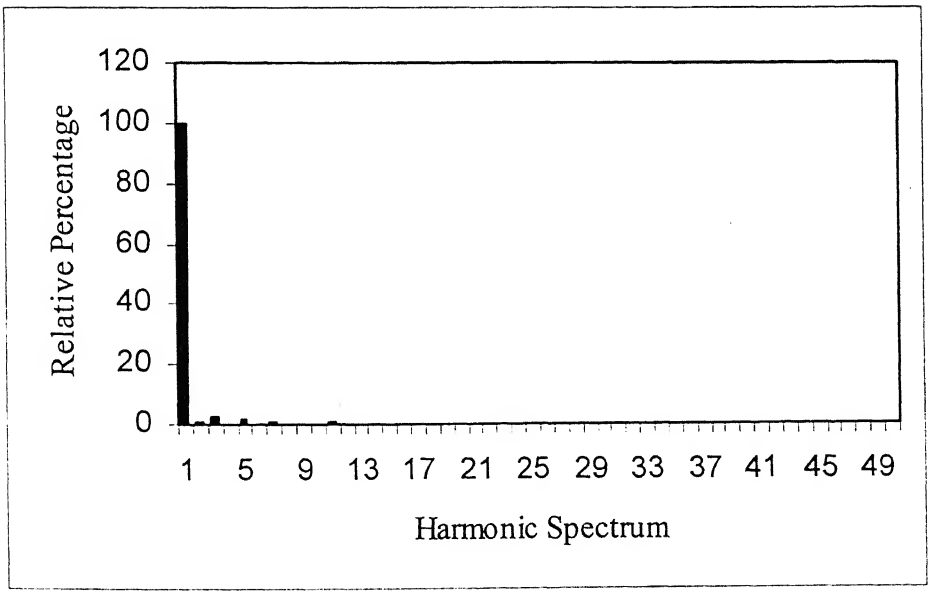

Fig. 3.24 Supply current (i_s) spectra (Experimental)

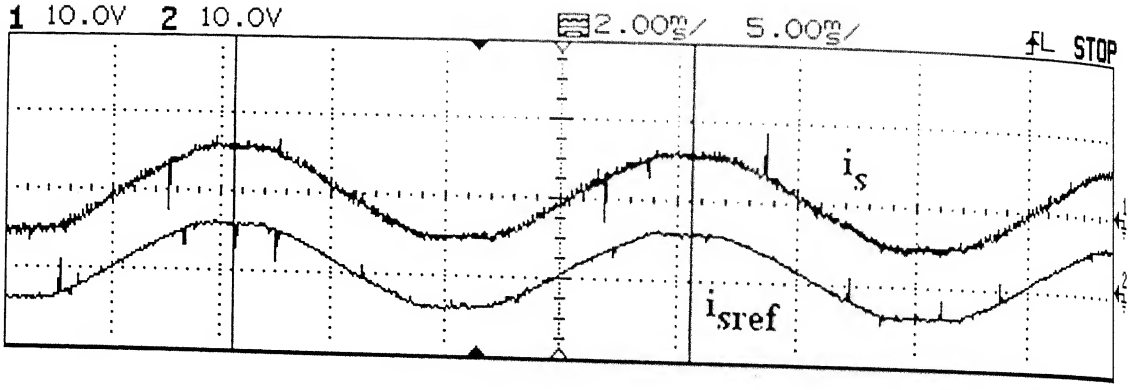

Fig. 3.25 Experimental results of supply current (i_s) and supply current reference (i_s^*)
X axis : 5 ms/div Y axis: 10 A/div

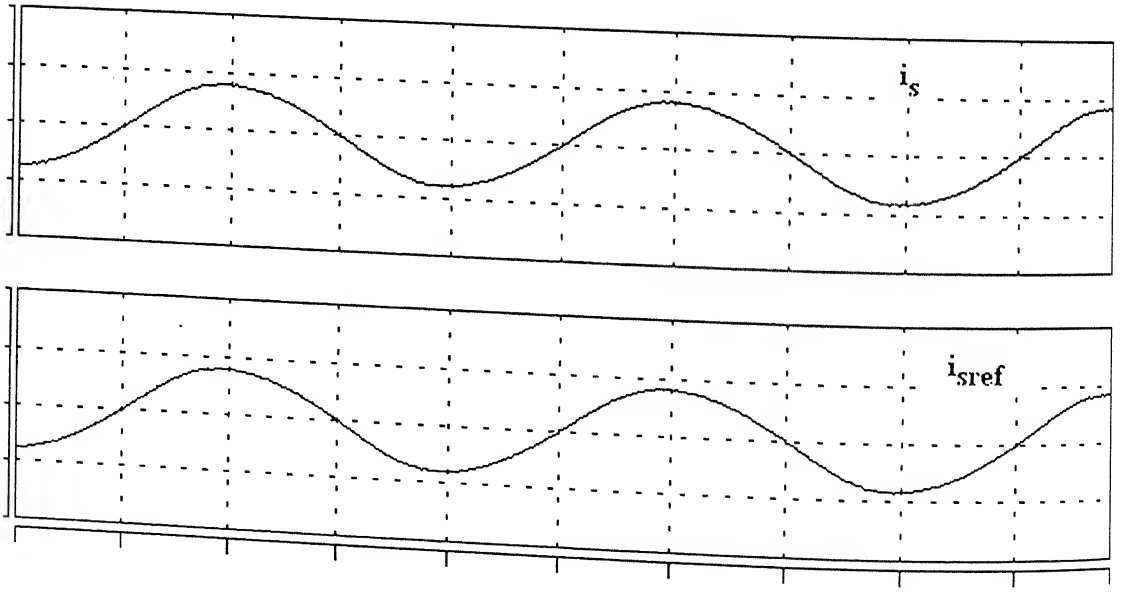

Fig. 3.26 Simulation results of supply current (i_s) and supply current reference (i_s^*)
X axis : 5 ms/div Y axis: 10 A/div

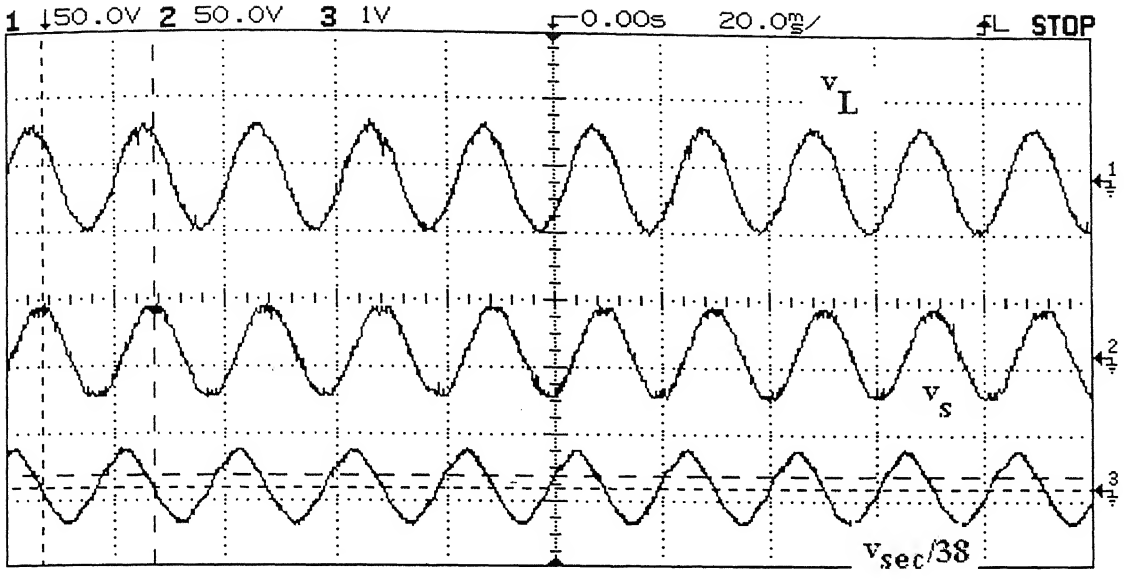

Fig. 3.27 Experimental result of v_L, v_s and vsec

Trace-1: Load voltage (v_L) y axis : 50 v/div

Trace-2: Supply voltage (v_s) y axis : 50 v/div

Trace-3: Series injected voltage (vsec) /38. y axis : 1 v/div

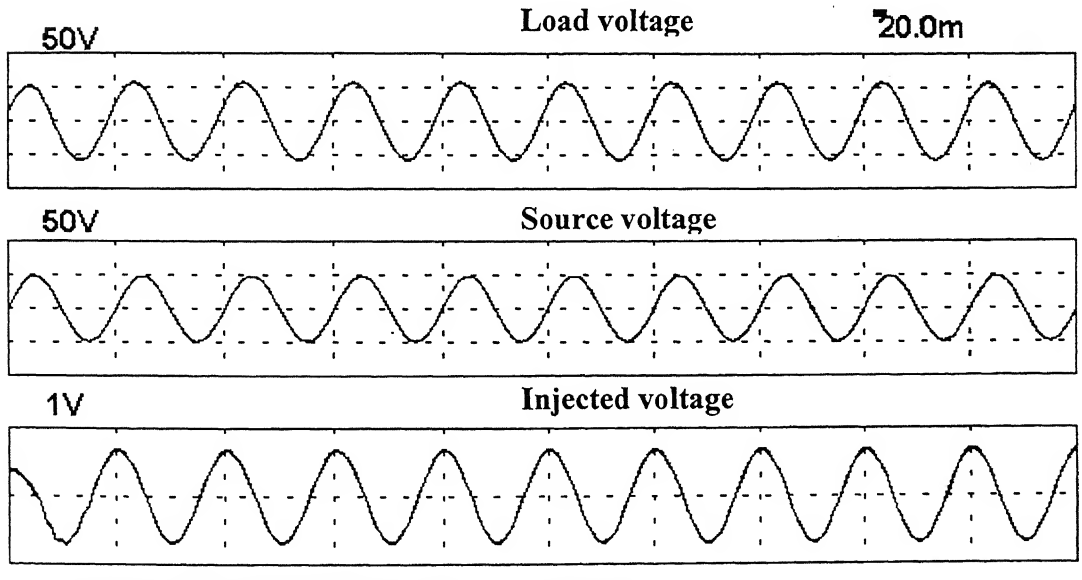

Fig. 3.28 Simulation result of v_L, v_s and vsec

Trace-1: Load voltage (v_L) y axis : 50v/div

Trace-2: Supply voltage(v_s) y axis : 50v/div

Trace-3: Series injected voltage (vsec) /38. y axis : 1v/div

3.8.2 Dynamic performance

The dynamic performance of UPQC has been studied in this section. Fig. 3.32 shows the transient response of UPQC when load current has an increment of (1.8 A – 2.5 A) by changing the dc side load resistance of the diode bridge rectifier. It is seen that the supply current remains within the specified band at every instant. Fig. 3.33 shows the corresponding simulation results.

Due to the transformer resistance, leakage reactance drop and the filter phase shift, a small amount of injected voltage is required to be introduced with a low modulating index of 0.4 in the nominal supply voltage condition. According to the requirement of voltage drop to be compensated during sag, the modulation index is adjusted appropriately. Voltage sag of 8% is created and it can be seen that the secondary injected voltage from the series compensator (SC) appropriately shoots up (trace 2 in Fig. 3.34) to maintain the load voltage (trace 1) at the desired level.

The details of the transients, as obtained from simulation, are given in Fig. 3.35. As the sag is created immediately after peak of the supply voltage (i.e. control delay is maximum), the load voltage dips from 54 V to 49 V volt, but as the controller takes fast action, the SC injects the additional voltage required, and the load voltage retrieves its desired value within next cycle, with nominal transient overshoot to 55 V. When the supply voltage sag is eliminated, i.e. the supply voltage regains its original value, there is a transient overshoot in the load voltage as the control signal takes maximum delay of 10ms for corrective action.

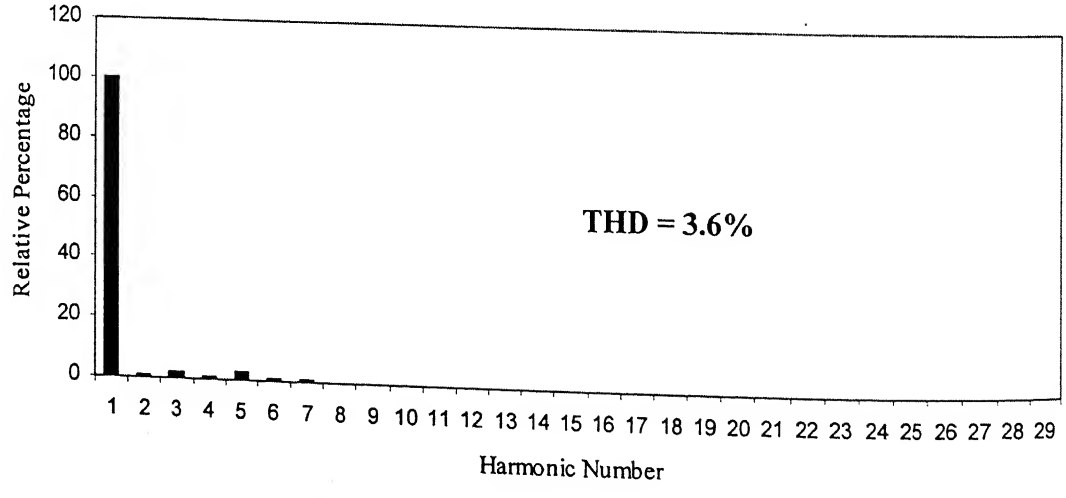

Fig. 3.29 Load voltage (v_L) spectra

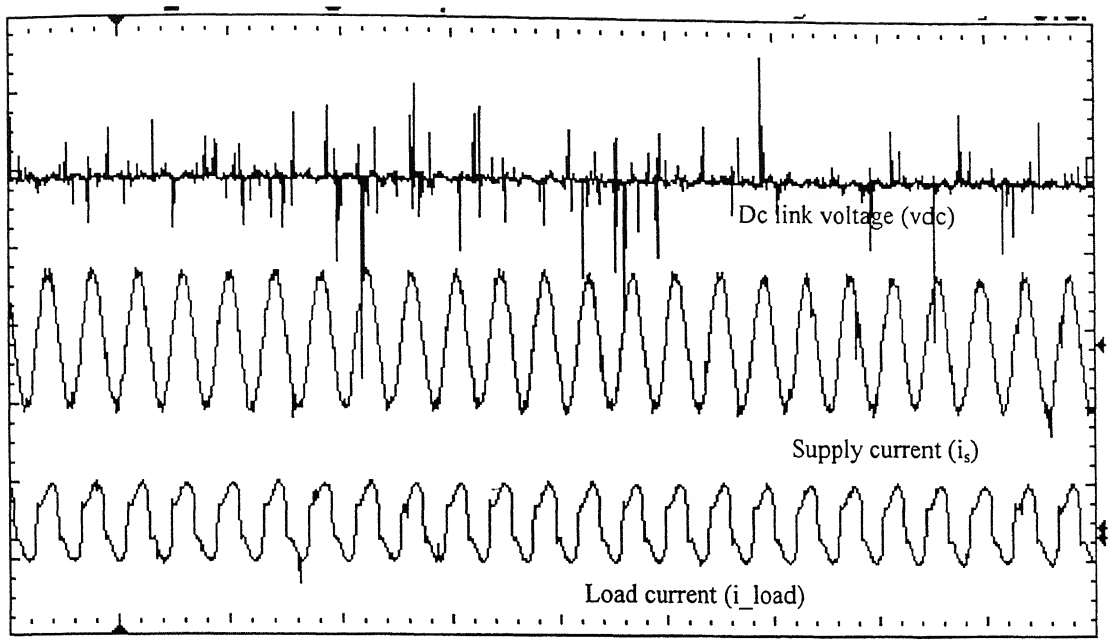

Fig. 3.30 Steady state experimental results of DC link voltage (Vdc), supply (i_s) and load current (i_L)

X axis : 50ms/div Y axis : vdc 20V/div, i_s, i_L 5A/div

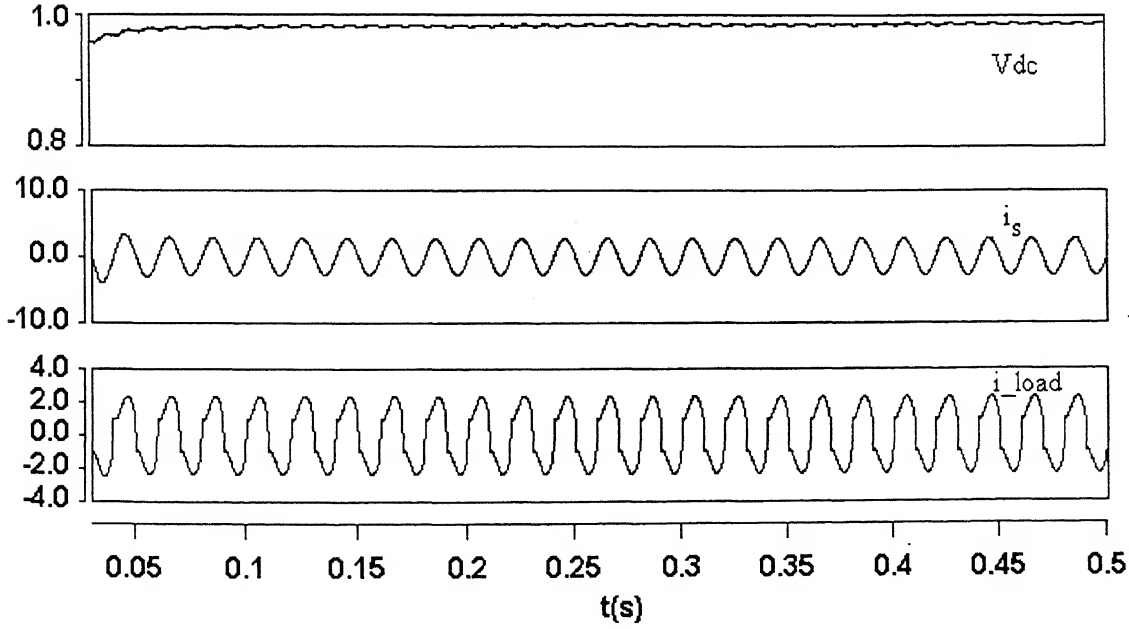

Fig. 3.31 Steady state simulation results of DC link voltage (Vdc/1000), supply (i_s) and load current (i_L)

X axis : 50 ms/div Y axis : Vdc .1 V/div, i_L = 2 A/div , i_s = 10 A/div

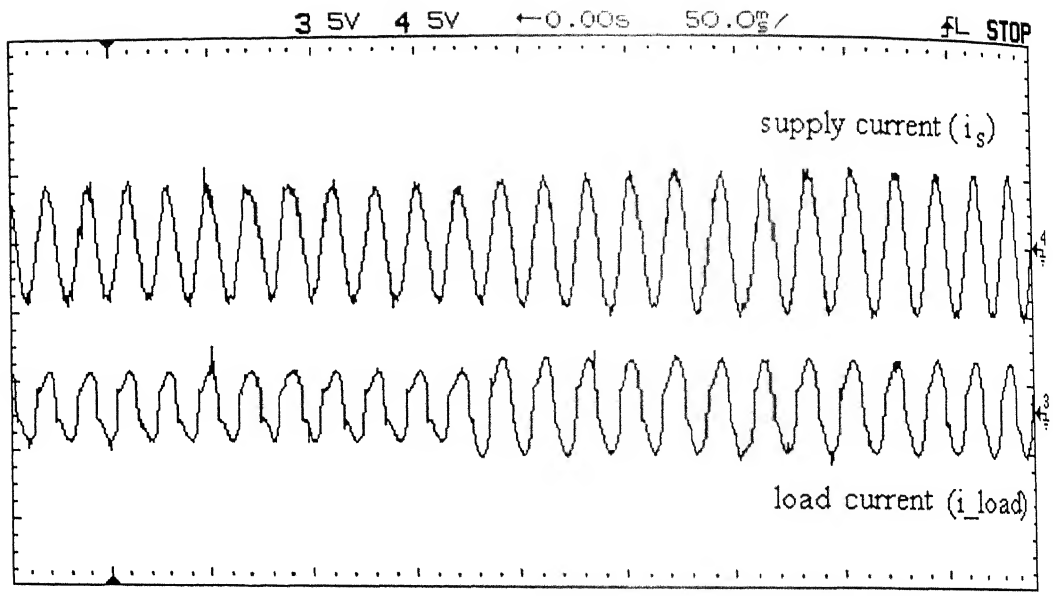

Fig. 3.32 Experimental results of dynamic load change

X axis: 50ms/div, Y axis: 5A/div

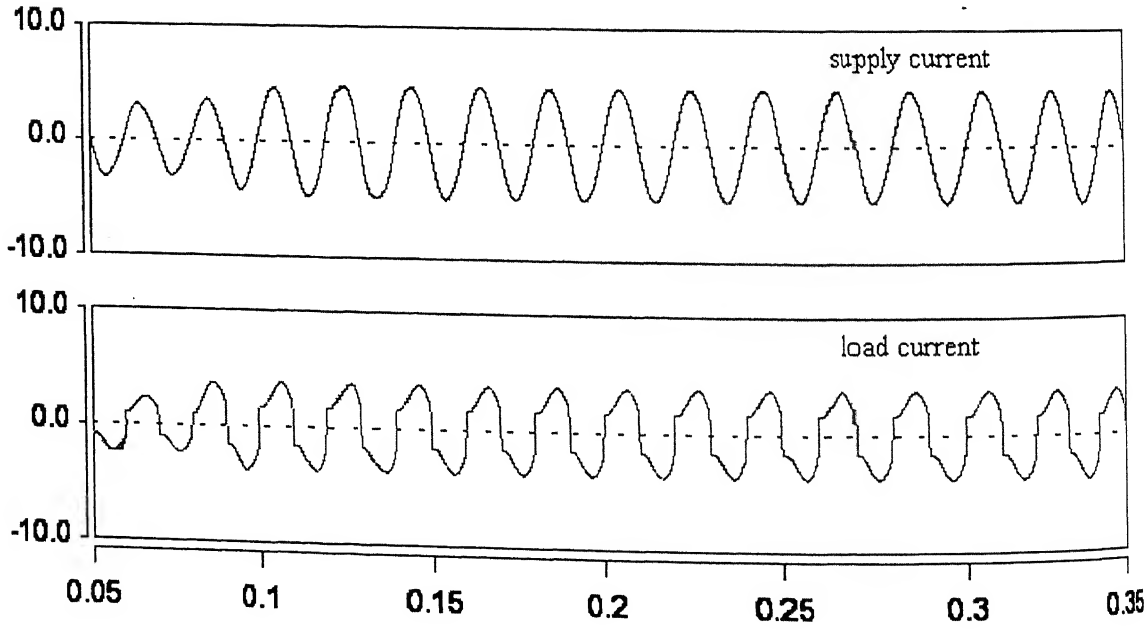

Fig. 3.33 Simulation results of dynamic load change

X axis: 50ms/div, Y axis: 10 A/div

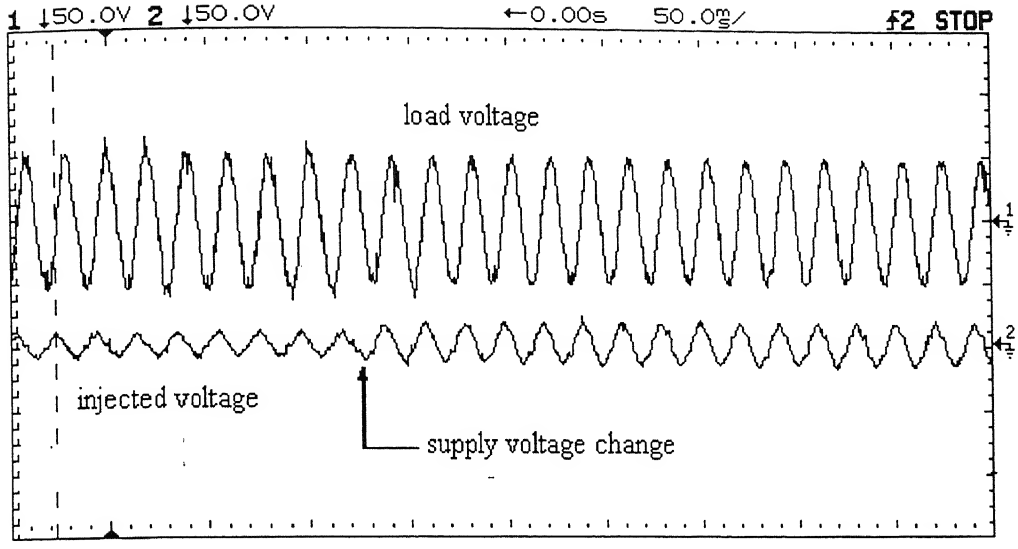

Fig. 3.34 Experimental profile of load voltage (v_L) and injected voltage (vsec), with a supply voltage change at the instant shown by an arrow

X axis: 50ms/div Y axis: 50 V/div

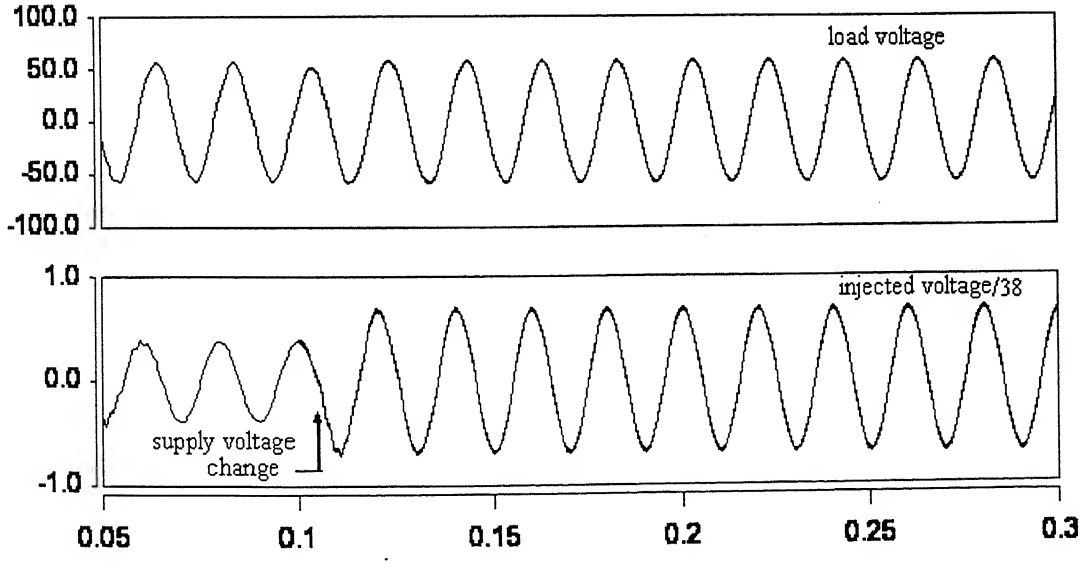

Fig. 3.35 Simulation profile of load voltage (v_L) and injected voltage/ 38 (vsec), with a supply voltage change at the instant shown by an arrow

X axis: 50ms/div Y axis: 50 V/div for v_L, Y axis = 1 V/div for vsec/38

3.9 Conclusion

The study of a single phase UPQC-Q for non-linear load has been reported in this chapter. The details of loading analysis have been carried out to determine the rating of the UPQC-Q. A new control strategy for single phase scheme has been developed, and it has shown its effectiveness in supply current wave shaping and maintaining input unity power factor at all conditions of load. The dynamic sag controller of UPQC-Q effectively maintains the load end voltage to its desired level. Depending on the dc link voltage, certain percentage of supply voltage sag can be mitigated. As UPQC-Q has a self supporting dc link voltage control scheme, it can cater to under voltage for any amount of time.

A novel hybrid controller has been used by effectively combining analog and digital control. The fast acting hysteresis current controller has been chosen to be analog, as the current reference profile can be traced accurately with good band-width, and digital circuit delay does not deteriorate the performance.

The dc link voltage controller is a relatively slower controller. To have the flexibility in parameter gain choice, it has been implemented in software inside PC. The dynamic sag controller has also been implemented inside PC, as several arithmetic calculations are required to be performed with a small sampling time.

Detailed performance analysis has been carried out in SABER simulator. A small scale laboratory prototype has been developed and tested. The results show good performance of UPQC. This study of single phase UPQC is of great importance in the design of three phase UPQC-Q, which is discussed in the next chapter.

Chapter 4

Three Phase Unified Power Quality Conditioner

4.1 Introduction

Most large power and industrial loads are three phase in nature. As discussed in Chapter 1, production industries like automobile manufacturing plants, paper mill, textile fibres, medicines, food production and processing, etc. have critical loads, which are sensitive to voltage variations and should be interested in a multi-purpose PQ compensating equipment. These loads require to avoid punitive tariff due to low power factor and THD, in addition to their protection from supply voltage variation. Hence, measures are taken to save them from production loss and also to maintain quality control.

This aspect brings out the importance of the investigations on three phase Unified Power Quality Conditioner (UPQC), which takes care of supply voltage sag in addition to compensating load harmonics and reactive current.

The present chapter gives the detailed simulation and implementation of three phase UPQC. Initially, a three phase UPQC-Q topology is chosen for quadrature voltage injection. The approach described in Chapter 3 for the single phase case has been extended to a three phase system. However, the implementation of the control blocks are more involved and complicated. As the number of feedback signals increase, one more digital to analog card PCL-726 is required, besides PCL-208.

The second part of the chapter discusses the control scheme of UPQC-P for in-phase series voltage injection. A suitable control technique has been developed for UPQC-P, to help maintain the load voltage balanced at the desired value even if there is a supply voltage unbalance. Extensive simulation results are provided in support of the theory.

4.2 Power Circuit Configuration and Operating Principle

The three phase UPQC consists of two three phase inverters connected in cascade as shown in Fig. 4.1. The scheme is for a three phase three wire system. Ideally each phase represents similar circuit as in the single phase case; however, some points of difference arise by virtue of the interdependence of the three phases. Although individual phases handle VAR, it is well known that in a sinusoidal balanced three phase system, average as well as instantaneous VAR sums up to zero. Therefore, in the ideal case when the shunt converter is used to compensate for the fundamental active power only, the dc link need not carry any current at all. But in reality, dc link capacitor carries the ripple current, which is largely dependent upon the switching frequency of the converter. The dc link voltage has to be higher than the peak of the line to line voltage of the supply in order to achieve effective current control. The other criterion of choice of dc link voltage depends upon the voltage sag to be mitigated through the series converter. The higher of the two voltages is selected as the choice of dc link voltage.

The functions of shunt and series compensators remain the same as that in the single phase case.

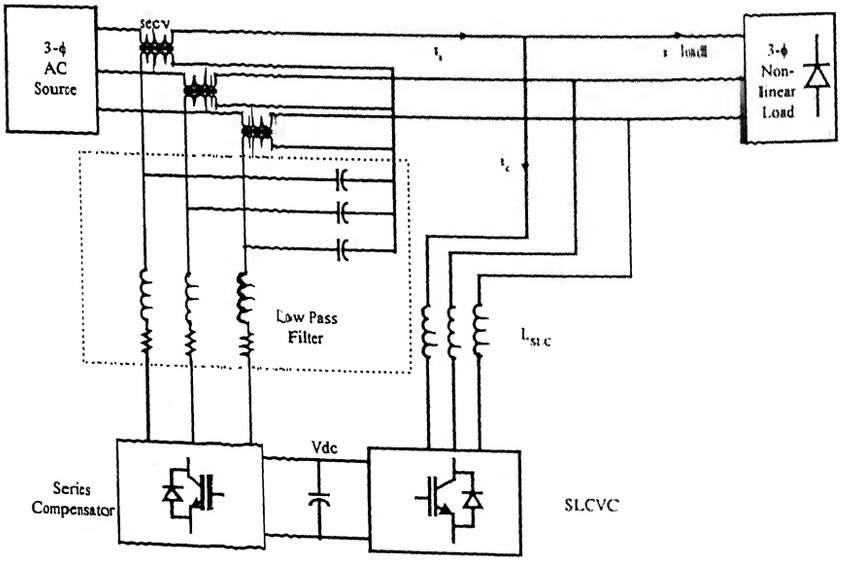

Fig. 4.1 Power circuit diagram of three phase UPQC

4.3 Control Strategy

The per phase control strategy of three phase UPQC-Q is same as that of the single phase UPQC-Q, which has been elaborated in Chapter 3, section 3.3. The shunt inverter (SLCVC) is a current controlled VSI. To keep the utility current sinusoidal and in phase with the respective phase voltage, the utility current is made to follow a suitable reference sinusoidal signal within a hysteresis band. In the event of a supply voltage sag, the series compensator takes action, and injects suitable voltage in quadrature advance to the utility current so that it does not consume any active power in the steady state. It also shares VAR of the load with the SLCVC. Like the single phase case, the dc link capacitor is shared by both the converters, and SLCVC maintains the charge of the dc link capacitor voltage through a closed-loop control.

The three phase UPQC-Q has four main control blocks, namely,

Controller of dc link voltage

Current controller for SLCVC

Dynamic sag controller

and *PWM voltage controller* as discussed in Chapter 3. The detailed hardware implementation has been elaborated in Section 4.5.

4.4 Simulation of UPQC-Q at Indian Distribution Level Voltage

The three phase UPQC-Q with its control scheme has been simulated in SABER. The results show satisfactory performance for non-linear load compensation and supply voltage sag mitigation.

Figs. 4.2 to 4.4 show steady state voltage and current for each phase. It is found that SLCVC of the UPQC is capable of maintaining unity input power factor. Fig. 4.5 shows the supply current, the load current and the SLCVC current of phase-A. Fig. 4.6 shows the load currents and the supply currents in all three phases. The supply currents are observed to be sinusoidal and balanced. It is found from Fig. 4.7 that THD of the load current is around 24% in each phase. After compensation, the supply current THD is brought around 5% (Fig. 4.8).

The dynamic performance under load change for phase A is observed in Fig. 4.9 and Fig. 4.10, where the load current (per phase) is increased from 12 A to 21 A (Fig. 4.9) and is reduced from 21 A to 12 A (Fig. 4.10). It is seen that at all instants unity input power factor is maintained. Fig. 4.11 shows the performance of UPQC under 20% supply voltage sag. It is seen that when the sag occurs, the load voltage also dips. But due to fast compensation, the load voltage is recovered completely in the next cycle. Depending upon the instant of occurrence of sag and restoration to original magnitude, there is a transient in load voltage due to the delay introduced by the peak detector circuit. In the result presented, the maximum undershoot at the time of sag is 14.7% in phase A and when the voltage is restored, maximum overshoot is 15% in phase-A of the load voltage.

At the time of injection of series voltage, THD in load voltage is found to be around 4% (Fig. 4.12), and this is well within the IEEE specified limit of 5%.

Fig. 4.13 shows the dynamic change in SLCVC current in phase A under supply voltage sag. As described earlier in Section 3.3, the condition refers to the phasor diagram of Fig.3.3c ($\theta > \phi$).Therefore to control the leading load power factor, the SLCVC current has to be lagging during sag compensation.

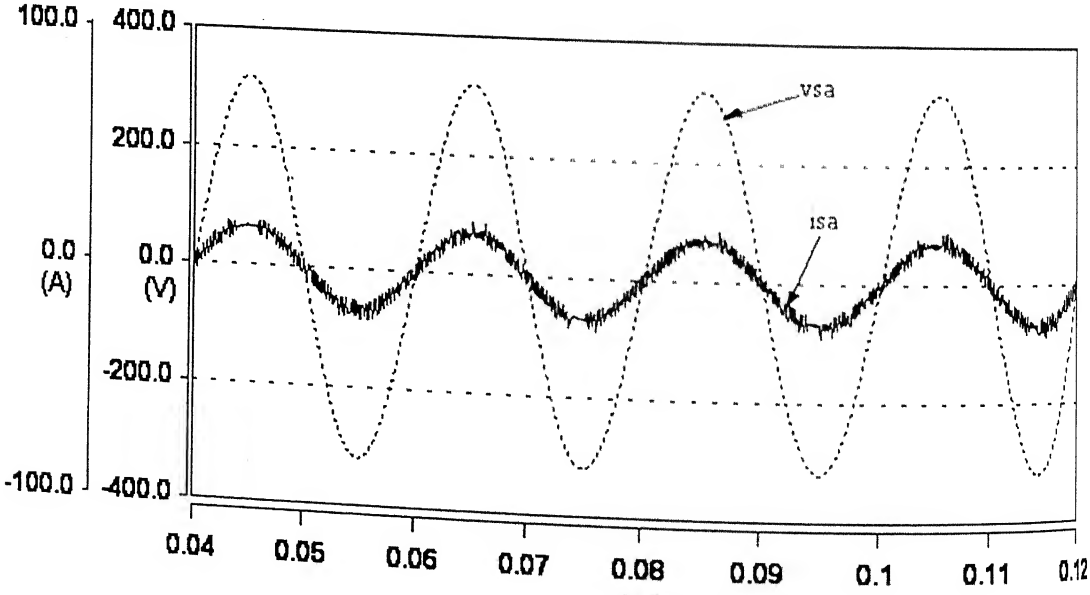

Fig. 4.2 Steady state voltage and current of supply phase-A

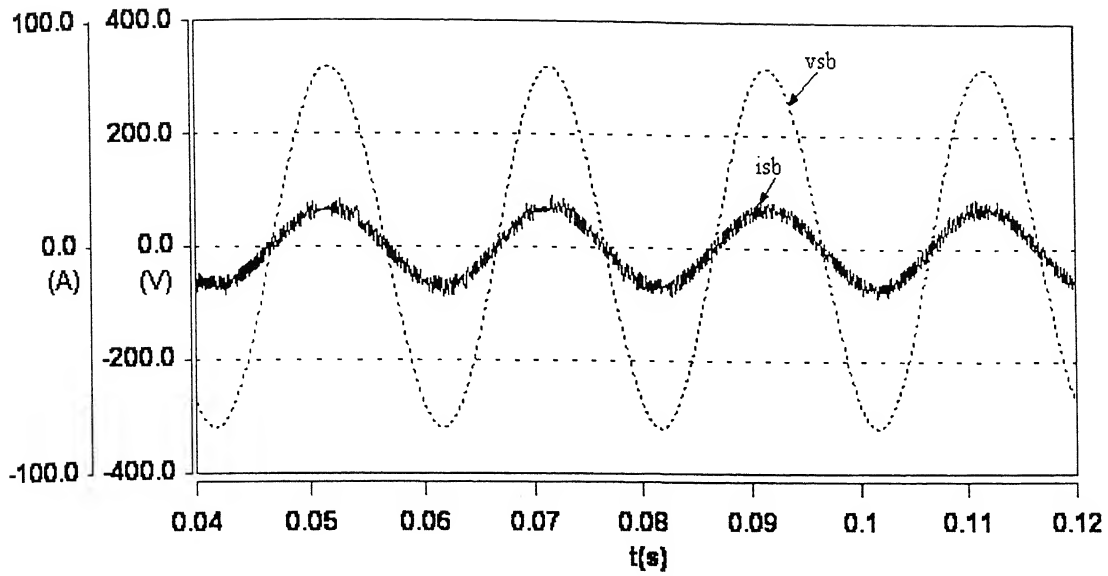

Fig. 4.3 Steady state voltage and current of supply phase-B

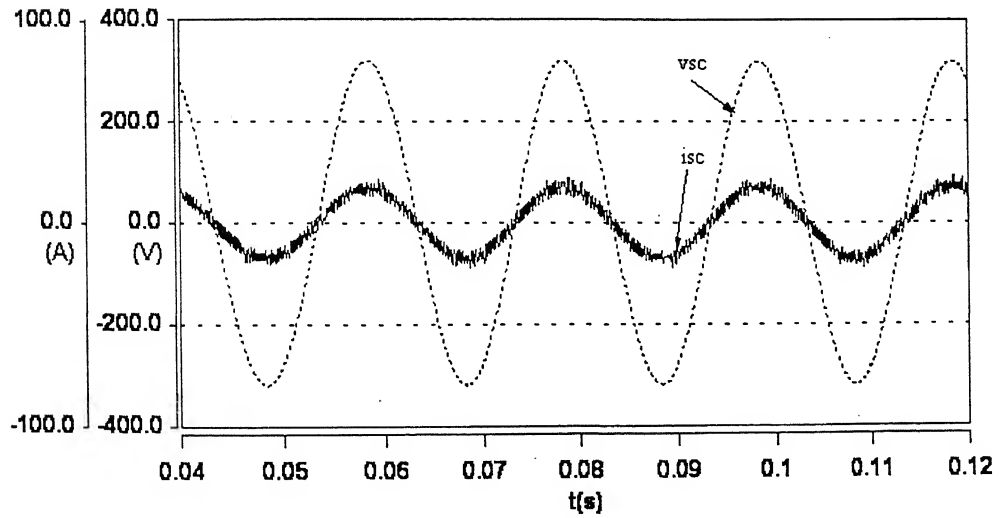

Fig.4.4 Steady state voltage and current of supply phase-C

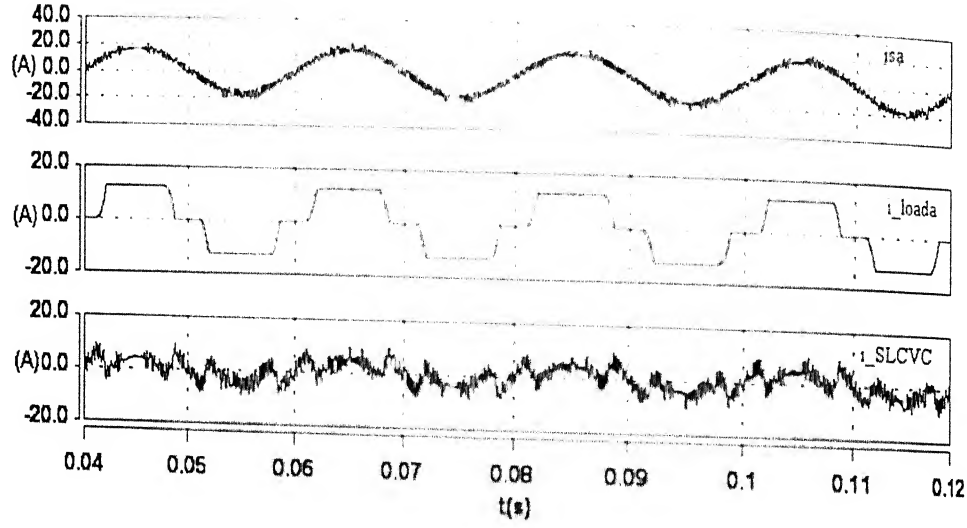

Fig. 4.5 Supply current, load current and SLCVC current of phase A

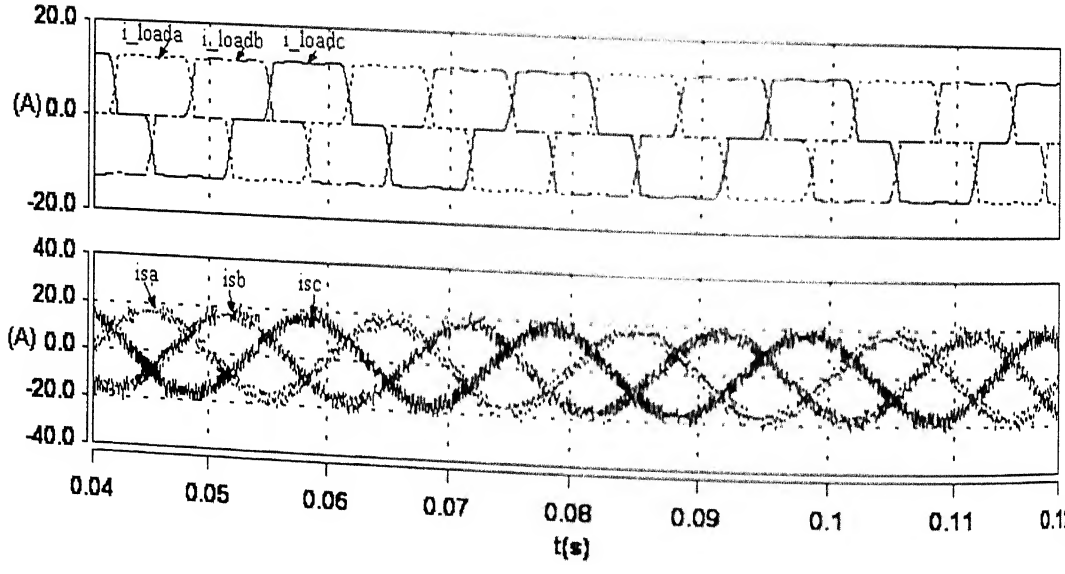

Fig. 4.6 Three phase load and supply currents

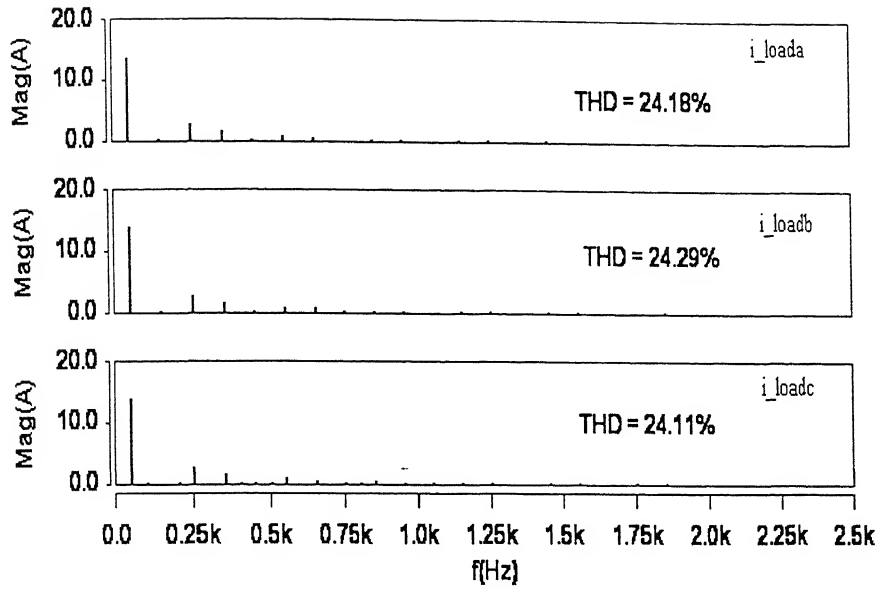

Fig. 4.7 Harmonic spectra of load current

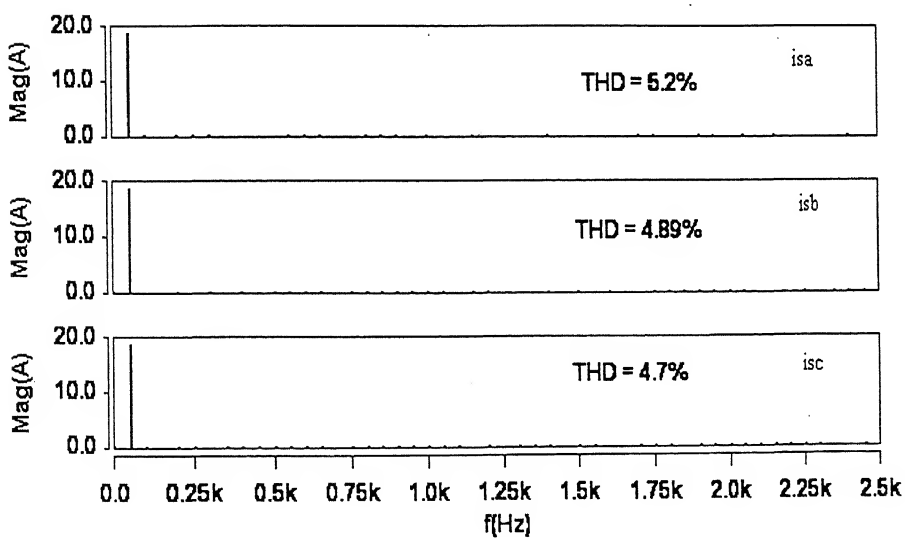

Fig. 4.8 Harmonic spectra of supply currents

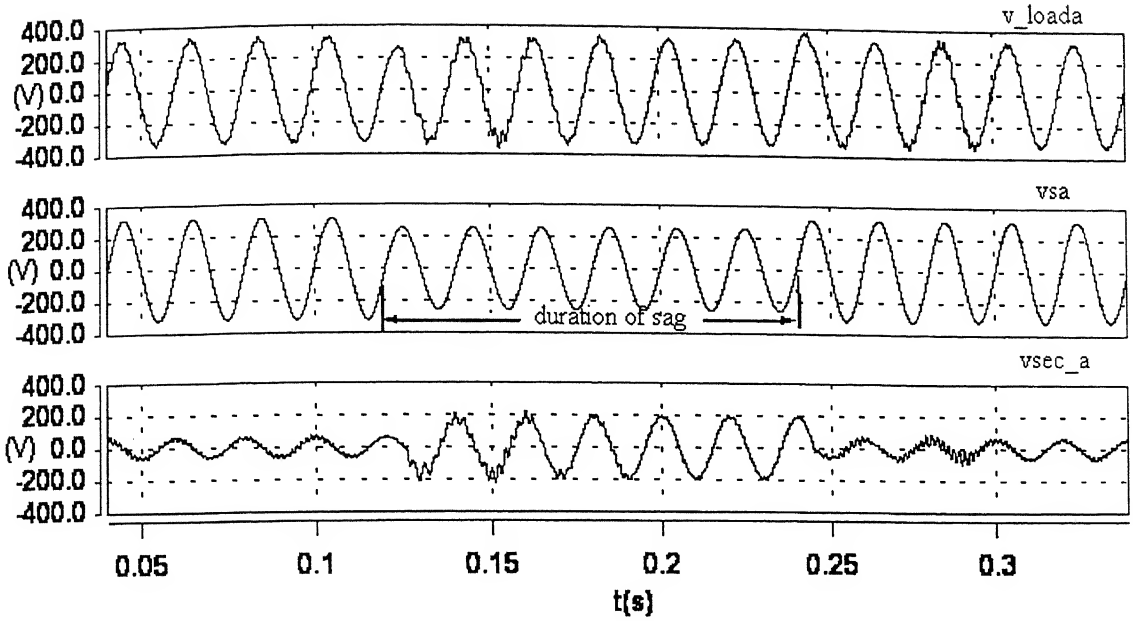

Fig. 4.11 Load, supply and injected voltages of phase A, under normal and 20% supply voltage sag condition

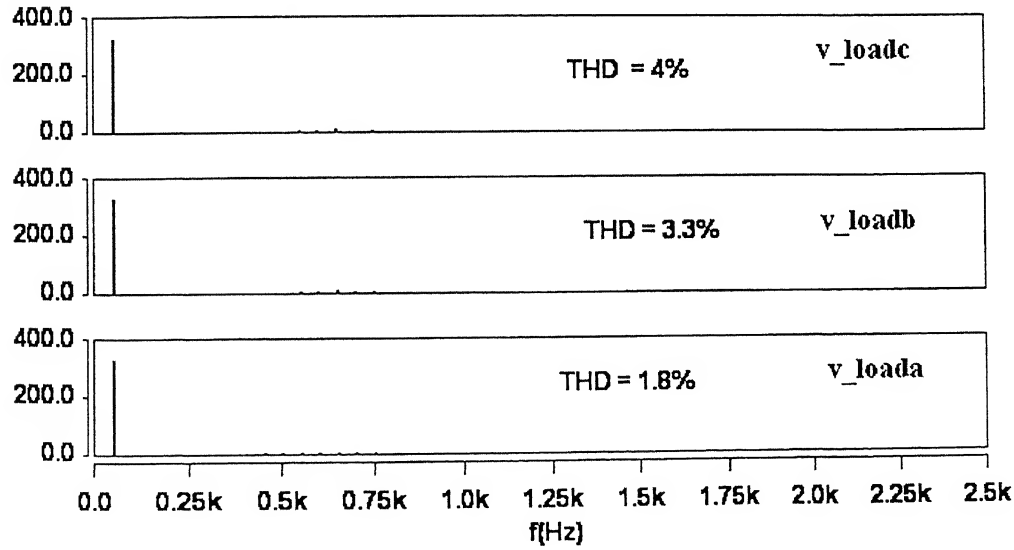

Fig. 4.12 Harmonic spectra of load voltages

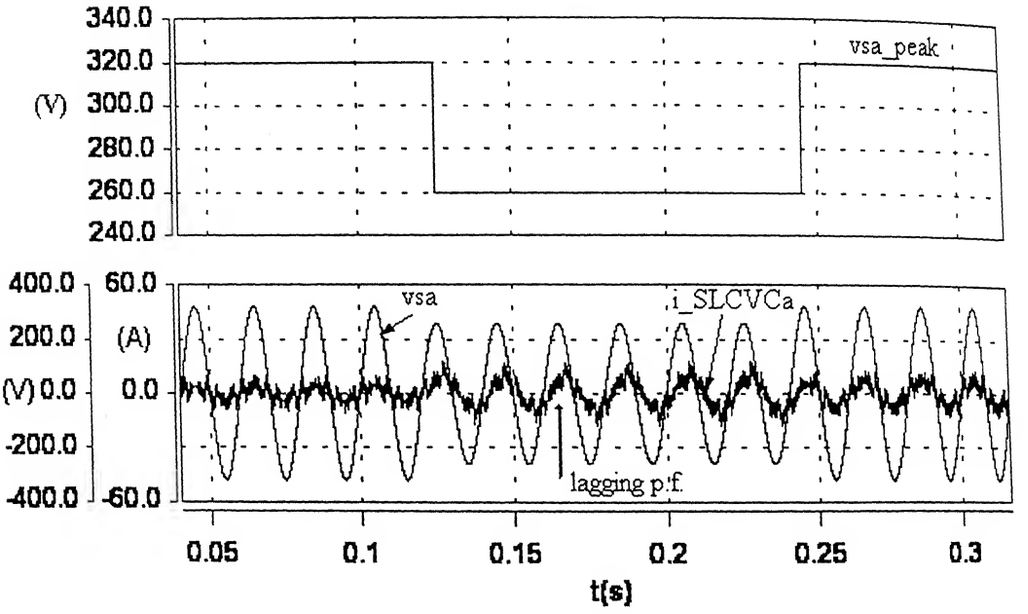

Fig. 4.13 SLCVC current of phase-A under normal and 20% sag condition

4.5 Implementation of Control Circuit

After extensive simulation of the proposed system, a laboratory prototype of the UPQC for experimentation has been designed and fabricated. Some of the components have been chosen according to the availability, and the aim has been to qualitatively verify the proposed control philosophy.

The control circuit is hybrid in nature, partly implemented with analog circuits and partly with digital ones using a Pentium–II PC @333 MHz, PCL-208 and PCL-726 (DAC) data acquisition cards. This implementation helps in achieving smaller sampling time. Fig. 4.14 shows the block diagram for experimental realization of the three phase control scheme. Analog and digital circuits are built in modular cards. Working aspects of a few typical blocks and their actual circuit implementation are discussed in the following sections.

The hysteresis controller for each phase is similar to that mentioned in Section 3.7.1, and is not elaborated any further. The point to be mentioned here is that the two reference supply current signals for phase-A and phase-B come out form the analog channel DAC_4 and DAC_5 of PCL-726. These two channels take external references (corresponding phase voltages) and they are attenuated with a suitable attenuating factor inside PC based on the required amplitude of per phase supply current. For a three phase three wire system, the third phase reference is obtained by adding the other two reference signals with a negative sign, as summation of all three phase currents has to be zero at any instant of time.

The dc link voltage control also remains the same as described in Section 3.7.2. Here, PCL-208 channel 0 (AD0) has been used to sense the dc link voltage signal for software control.

The philosophy of dynamic sag controller remains the same as that in the single phase case. However due to mutually dependent signals, the control has been implemented in a manner so as to minimize the number of AD channels and to reduce the program execution time. A few typical control circuits of the three phase system are discussed in the following section.

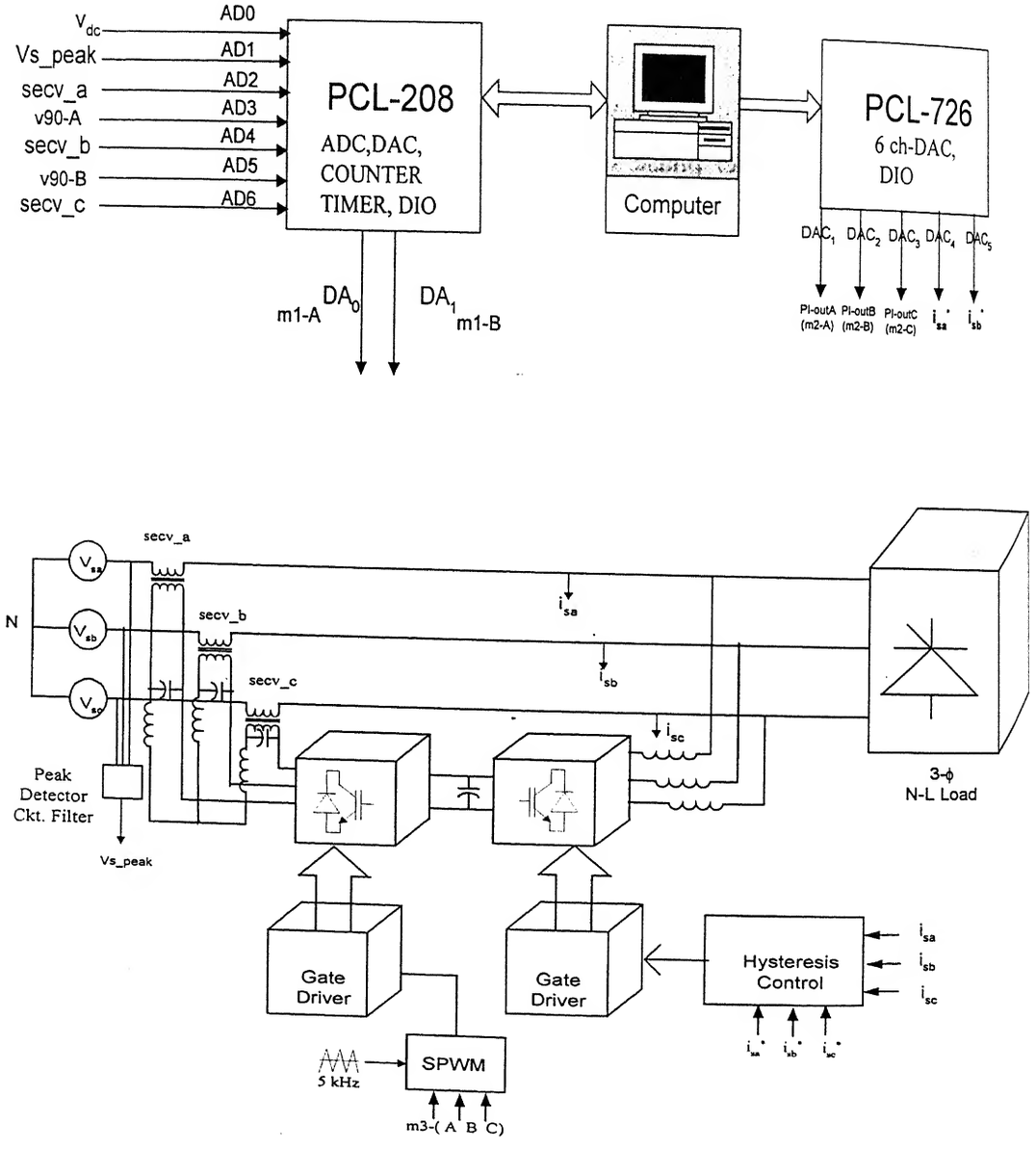

Fig. 4.14 Block diagram of hardware implementation of three phase UPQC-Q

4.5.1 Peak detector circuit

Assuming balanced supply voltage, the three phase voltages are scaled down and fed to a diode bridge rectifier and a 10 kΩ resistor is connected at the output, as shown in Fig. 4.15. The voltage across the resistor is passed through a LPF and the output gives a measure of the supply voltage peak, with a suitable multiplying factor. This eliminates the problem of accurate peak instant determination.

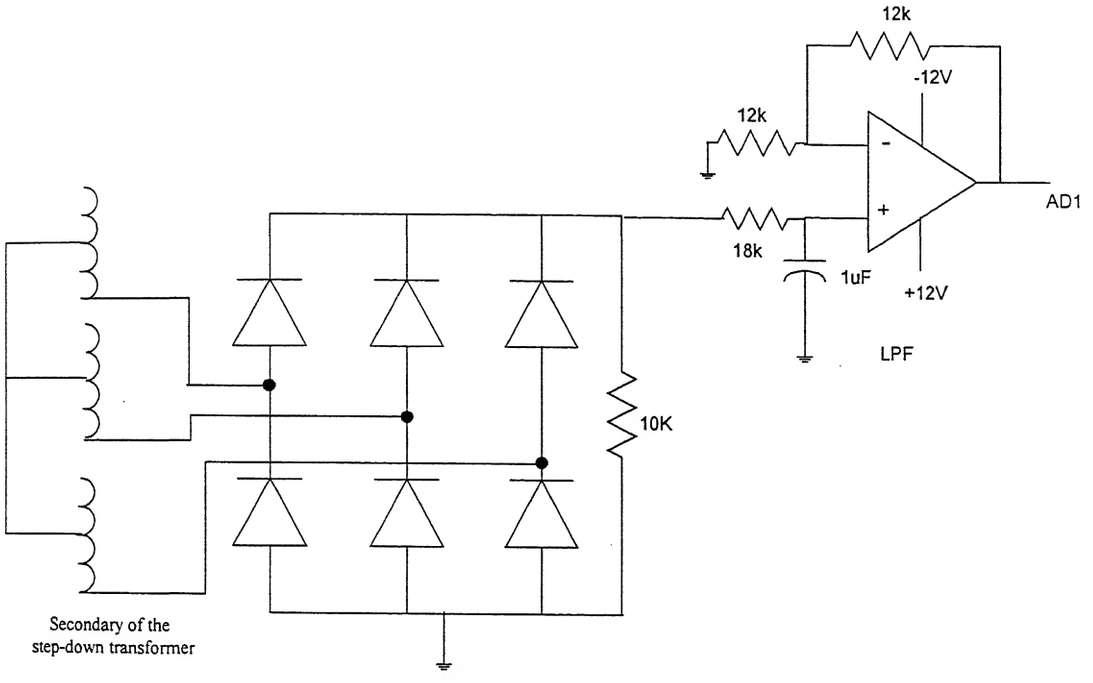

Fig.4.15 Supply voltage peak detector circuit

PCL-208 input

A high performance data acquisition card, PCL-208, manufactured by Dynalog Micro Systems, India, has been used for signal interfacing with the PC. The card has 16 analog input channels, two analog output channels, digital I/O, timer etc. The details of the card are given in the Appendix D.

PCL-726 output

PCL-726 is a 6 channel D/A card manufactured by Dynalog Micro Systems, India. Apart from 6 analog output channels, there are 16 D/I and D/O ports [69]. The details of the card is given in the Appendix E.

The use of these add-on cards for signal interfacing in various control blocks is described in the following few paragraphs. Fig. 4.16 shows the various analog signals interfaced through the PCL-208 AD data acquisition card. Figs. 4.17 a, 4.17b, 4.17c, 4.17d show the details of some typical analog circuit blocks shown in Fig. 4.16.

4.5.2 Dynamic sag controller block

Fig. 4.18 shows the control blocks used for dynamic sag controller per phase. As seen from the figure, the injected voltage in phase A (vsec_a) is sensed through a voltage sensor and a LPF, and sent to the AD ch-2 (AD2). The sinusoidal template in phase with phase-A voltage is phase shifted by 90° (v90-A) and is sensed through ch-3 of the ADC (AD3). It is then multiplied with a proper gain K inside the PC so that the signal becomes the reference injected voltage for phase-A ($vinj^*$-A). The actual injected voltage of phase-A is compared with $vinj^*$-A and the error is processed through a software PI controller, whose output is sent out of the PC through the other DAC card, PCL-726 ch-1 (DAC_1), and a LPF to generate a signal m2-A. Depending upon the filter phase shift, a 75° phase shifted sinusoidal template (v75-A) is multiplied with the modulation index in a DAC channel of PCL-208 (DA_0) and generates a signal m1-A. m1-A and m2-A are externally added with an analog adder to generate the final modulating signal for phase A of the series inverter (m3-A). This control scheme ensures fast and effective control of the series injected voltage.

4.5.3 SIN-PWM controller

Fig. 4.19 shows the three phase control circuit for sin-triangle comparison. The modulation signals are obtained from m3-A, m3-B, m3-C, as described in Fig. 4.18.

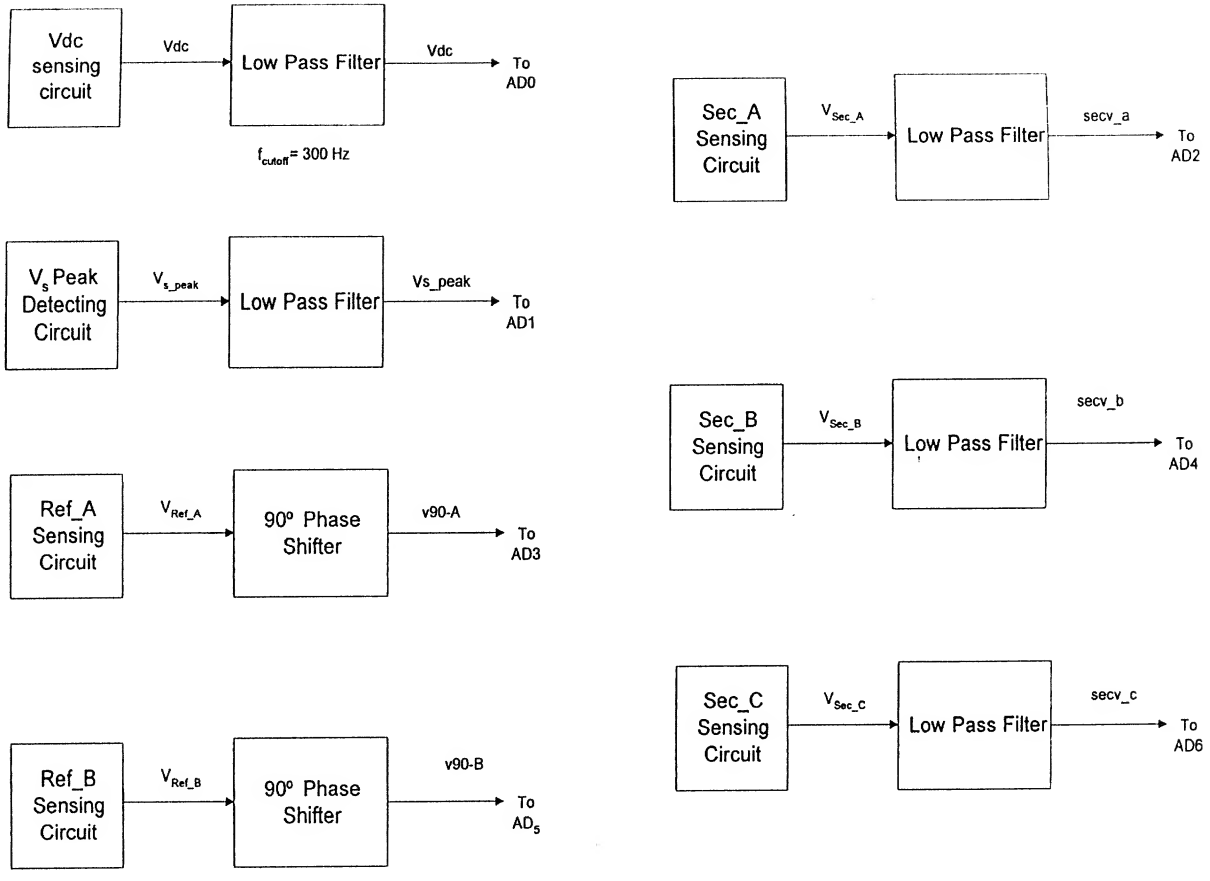

Fig. 4.16 AD interfacing block diagram for PCL-208

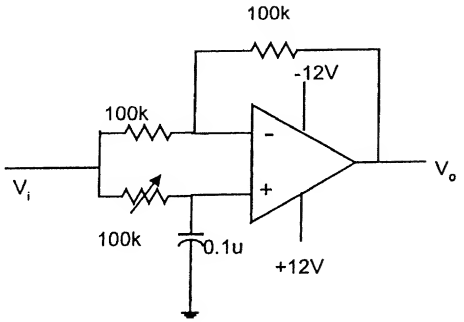

Fig. 4.17a 90 ° phase shifter

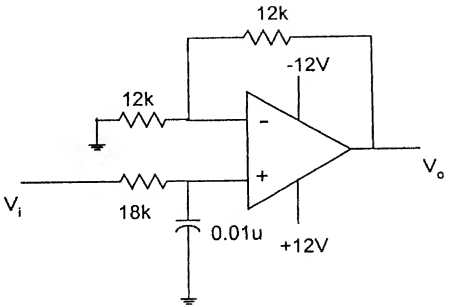

Fig. 4.17b Low pass filter
f_{cutoff} = 100 Hz

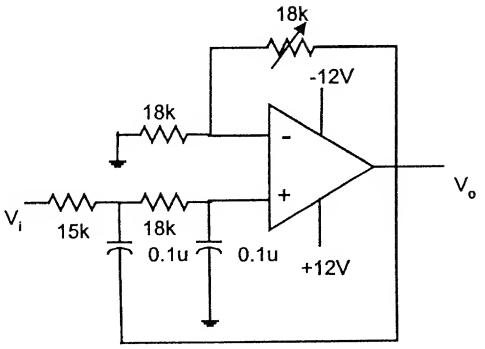

Fig. 4.17c Low pass filter
f_{cutoff} = 300 Hz

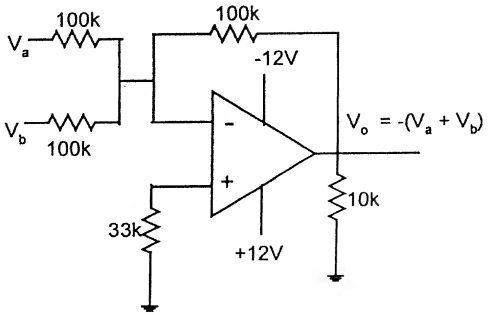

Fig. 4.17d Adder circuit

Fig. 4.17 Details of different analog circuits

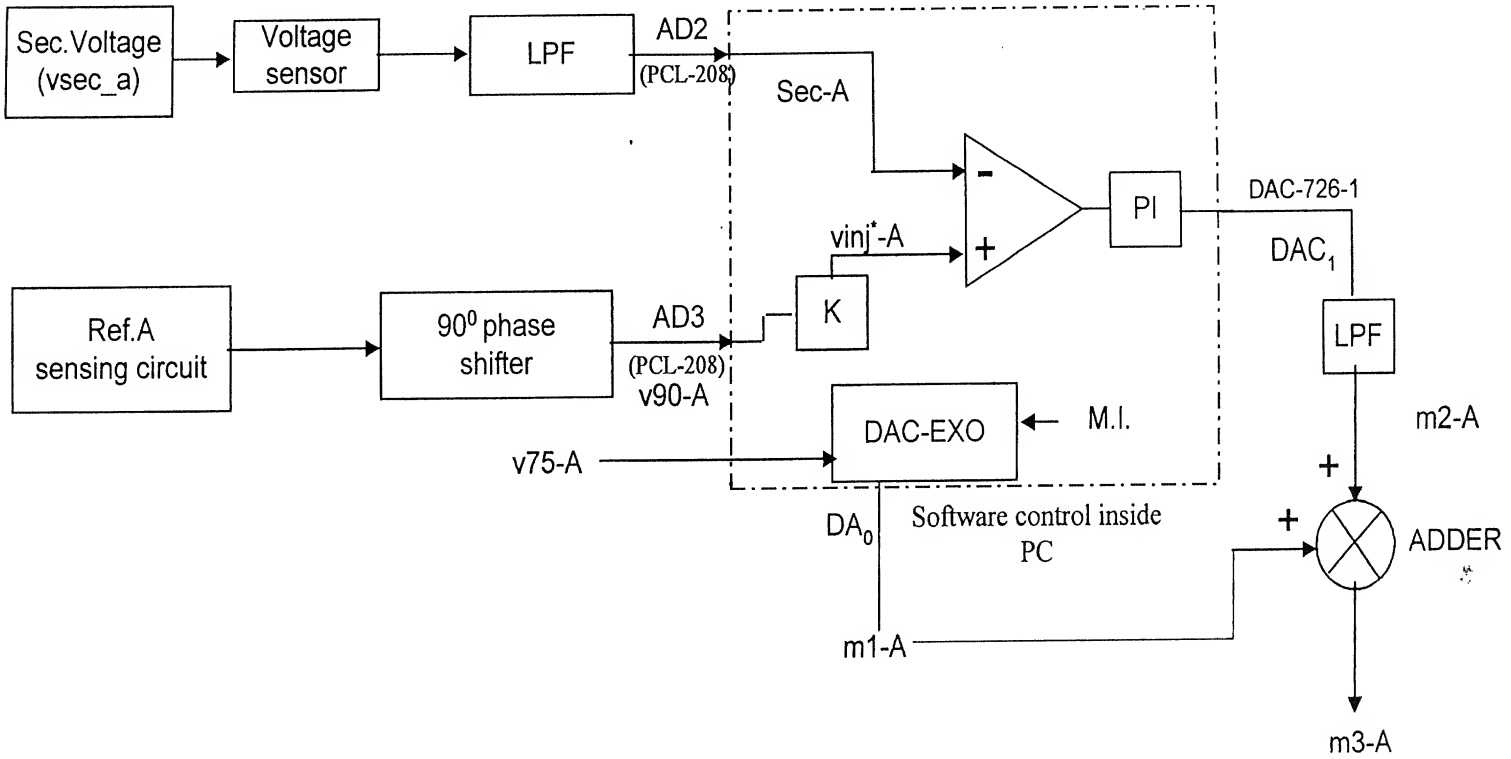

Fig. 4.18 Dynamic sag controller of phase-A

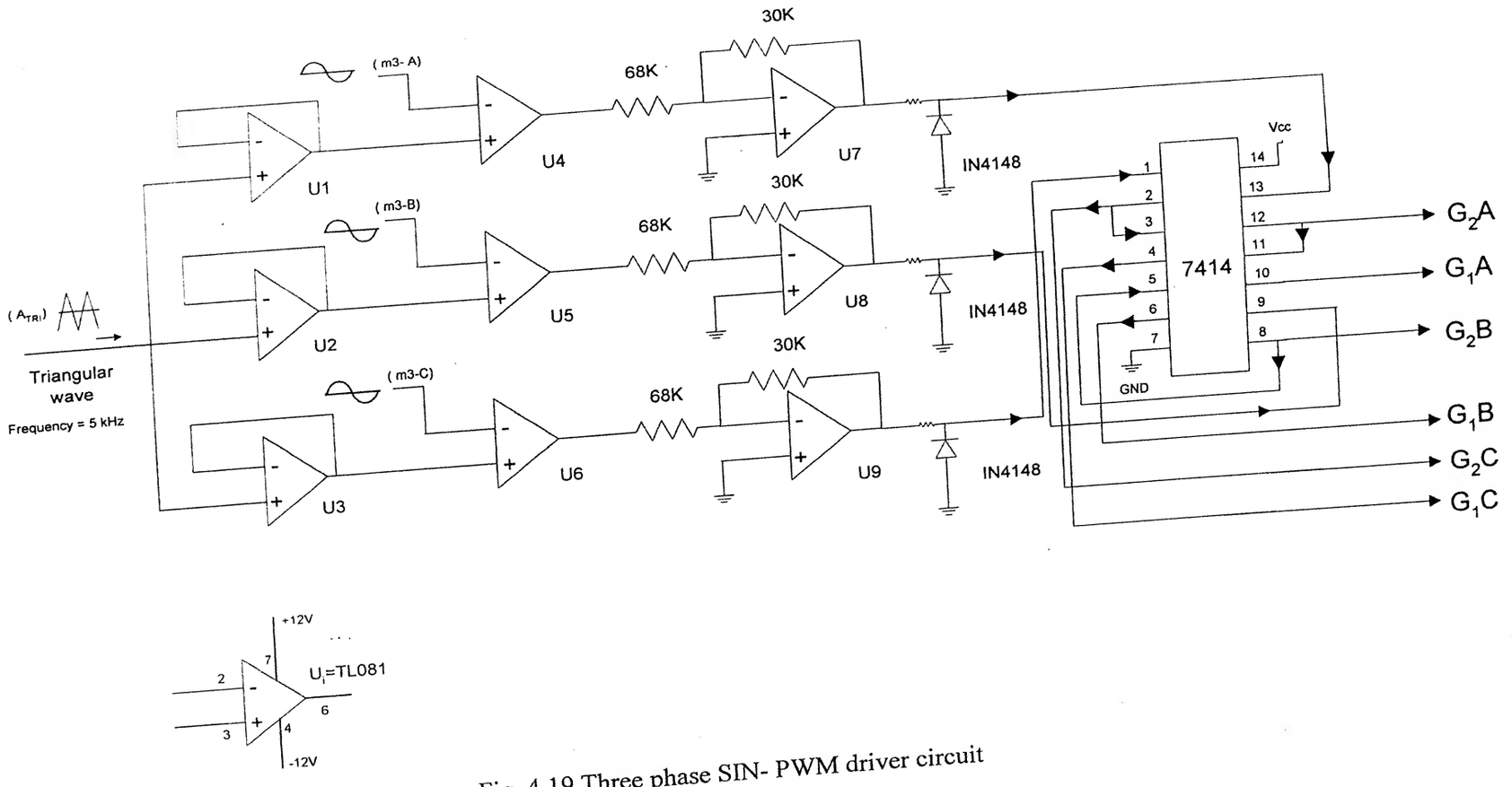

Fig. 4.19 Three phase SIN- PWM driver circuit

4.6 Experimental Validation

Some typical experimental results are presented in this section. The system parameters are given in Table 4.1. The PI controller gains of the dc link voltage control loop are $k_p = 1$ and $k_i = 0.1$ which has been found out by trial simulations. The trial was based on the performance of dc link voltage reaching its reference value and minimal transient oscillations respectively. In the dynamic sag controller, the feed-forward and the feed-back PI gains are $k_p = .002$, $k_i = 0.0005$, which are chosen for fast response, dynamic phase shifting performance, and minimum oscillation of sag controller.

The algorithm for real time coordinated control of UPQC is implemented in Turbo-C language; the computation of each cycle takes about 168 μsec. The sampling speed is found sufficient for successful operation.

Table 4.1 System Parameters

System Voltage	35 V rms
Synch. Link Inductor	4.3 mH, 0.6 Ω
DC Link Capacitor	2200 μF,400 V dc
Dc link voltage reference	110 V
Load Current	1.62 A – 2.14 A
Non-linear	
LPF parameter	
R= 0.6 Ω	
L= 4.2 mH	
C= 60 μF	
Transformer parameters	
Lp = 5.66 H	
Rp = 0.7 Ω	
Ls = 1.38 H	
Rs = 0.5 Ω	

The load current, source current, load voltage and source voltages from the experimental setup are reported here.

A three-phase diode bridge rectifier has been used as a non-linear load and the effect of change in load current is recorded for each phase. Fig. 4.20a (for phase A) shows a change in load current from 1.64 A to 2.14 A (24% change) per phase. Corresponding change in supply current is observed to be from 2.65 A to 3.5 A. The simulation result for the same condition is presented in Fig. 4.20b. Fig. 4.21a and Fig. 4.21b show experimental and simulation results of the supply voltage and supply current of phase-A when the load change, as mentioned above, occurs.

Table 4.2 gives the harmonic spectra of load current and supply current in phase-A. The measurement is done through a power analyzer (PM100R). It is observed from the table that the predominant harmonics in the load currents are 5^{th}, 7^{th}, 11^{th} and 13^{th}, and the THD of the load current is 23.28%. The table also shows that with the application of UPQC, the utility current THD has been brought down to 2.957%. The simulation analysis of phase-A current harmonics is shown in Fig. 4.22. The displacement factor has improved from 0.768 to 0.992.

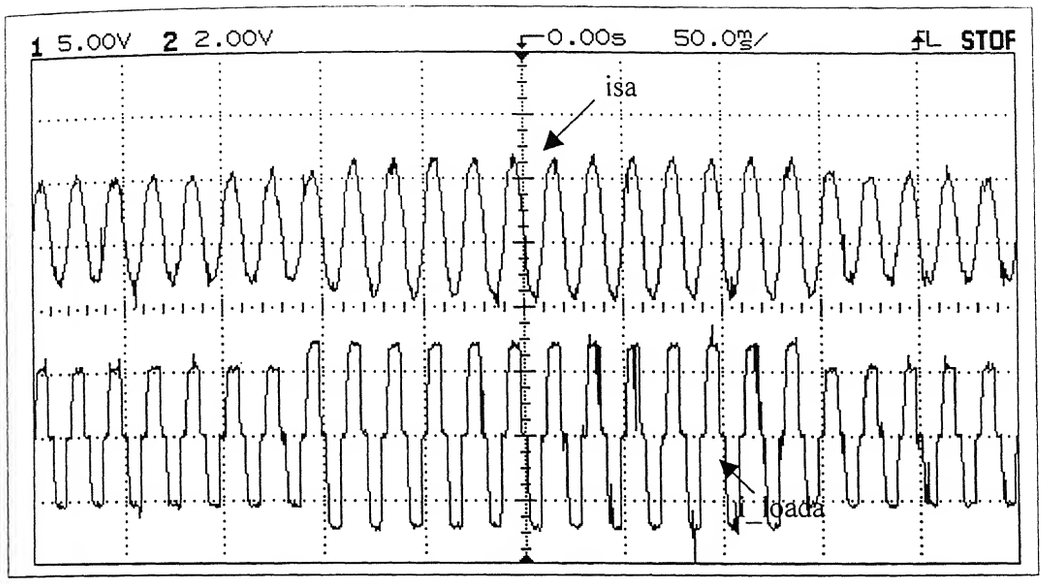

Fig. 4.20a Experimental results of supply current and load current of phase A

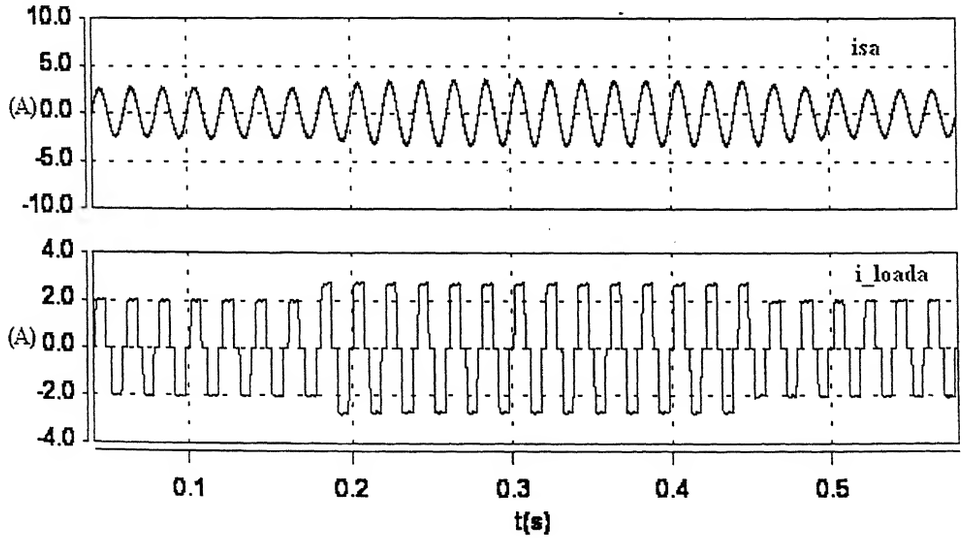

Fig. 4.20b Simulated results of supply current and load current of phase A

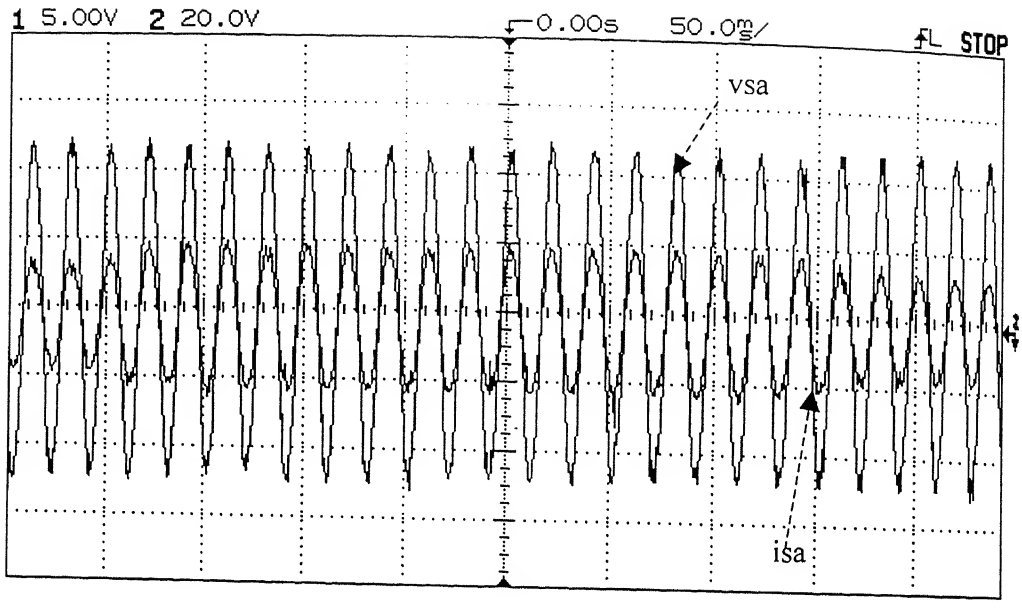

Fig. 4.21a Experimental results of supply current and supply voltage of phase A
X axis: 50 ms/div, Y axis: 5A/div for isa, 20 V/div for vsa

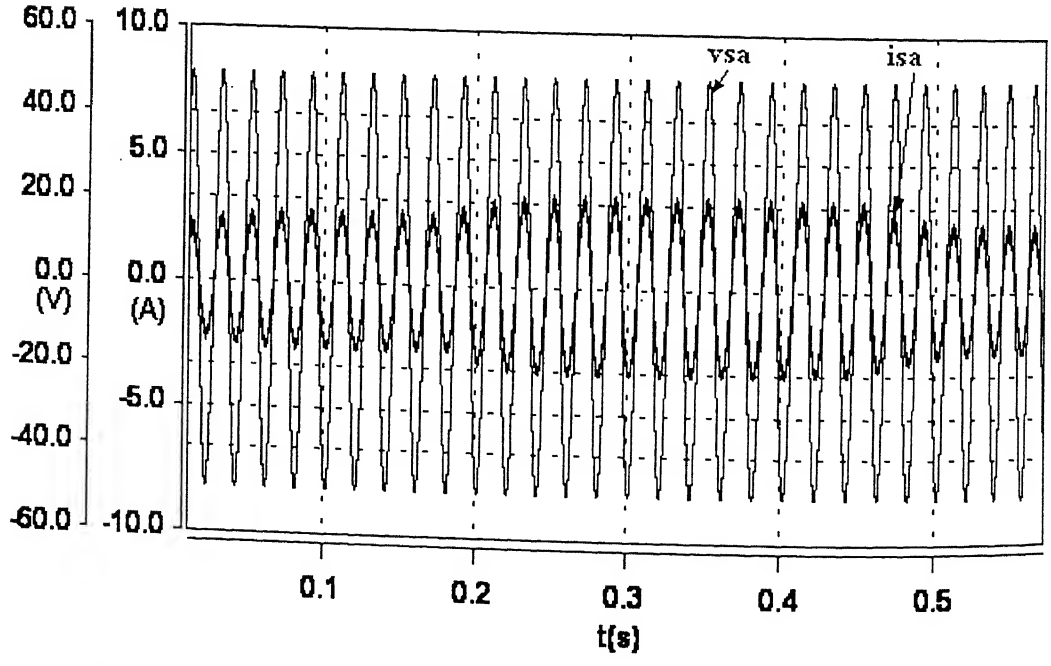

Fig. 4.21b Simulated results of supply current and supply voltage of phase A

Table 4.2

Harmonic spectra of load current and supply current of phase-A

Harmonic order	Load Current (A-phase)		Supply current (A-phase)	
	Magnitude	% fundamental	Magnitude	% fundamental
1st	1.645 A	100	2.652 A	100
5th	313.47 mA	19	38.989 mA	1.46
7th	204.86 mA	12.45	19.43 mA	0.73
11th	113.09 mA	6.87	23.4 mA	0.88
13th	80.05 mA	4.86	10.18 mA	0.38
17th	31.43 mA	1.91	16.68 mA	0.62
19th	28.13 mA	1.71	15.76 mA	0.59
23rd	13.674 mA	0.83	12.3 mA	0.46
25th	9.159 mA	0.5	10.1 mA	0.38
THD	**23.28%**		**2.957%**	
Displacement Factor	0.768		0.992	

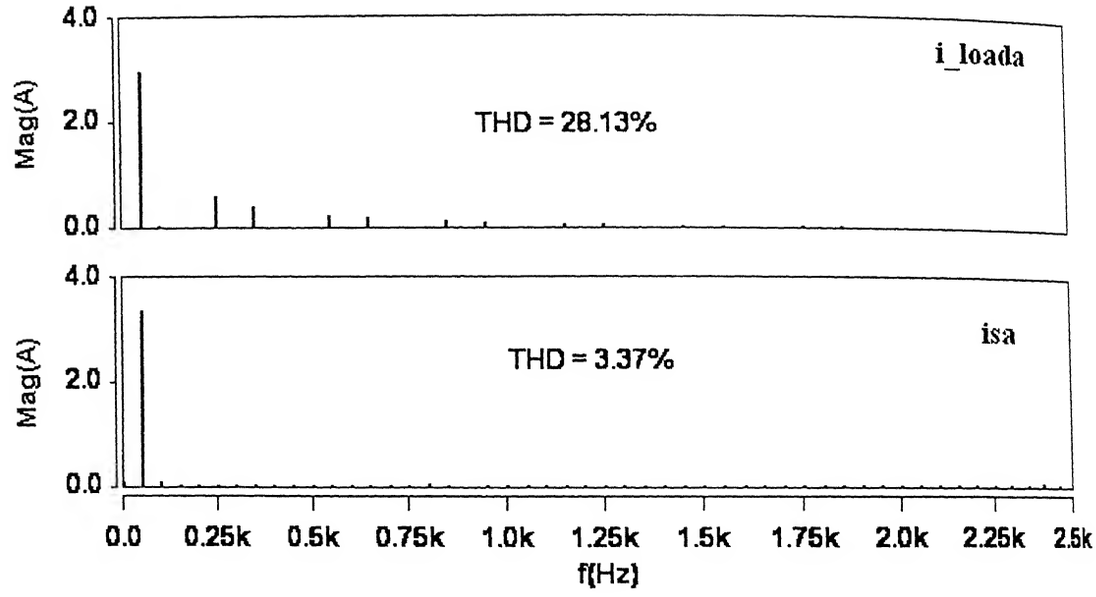

Fig. 4.22 Simulated results of harmonic spectra of load and supply currents in phase-A

The dynamic performance of UPQC-Q under supply voltage sag has been studied. Fig. 4.23a shows load voltage profiles of phase A, when there is a balanced 8% sag created in each phase. The sag has been created by switching on a three phase R-L load suddenly across the supply for a few cycles and switching it off to restore the original supply voltage. Due to laboratory limitation, deeper sag experimentally was avoided.

Simulation results for the same condition mentioned above are presented in Fig. 4.23b. The simulated result and experimented results match closely.

As described in the phasor diagram in Section 3.3, to maintain the active power balance, the supply current will increase during sag. This is verified experimentally as well as in simulation in Fig. 4.24a and Fig. 4.24b. The experimental and simulation results show the quadrature relationship between the supply voltage and injected voltage of the UPQC from Fig. 4.25a to Fig. 4.27b for each phase. The experimental results show the performance of the UPQC-Q satisfactorily.

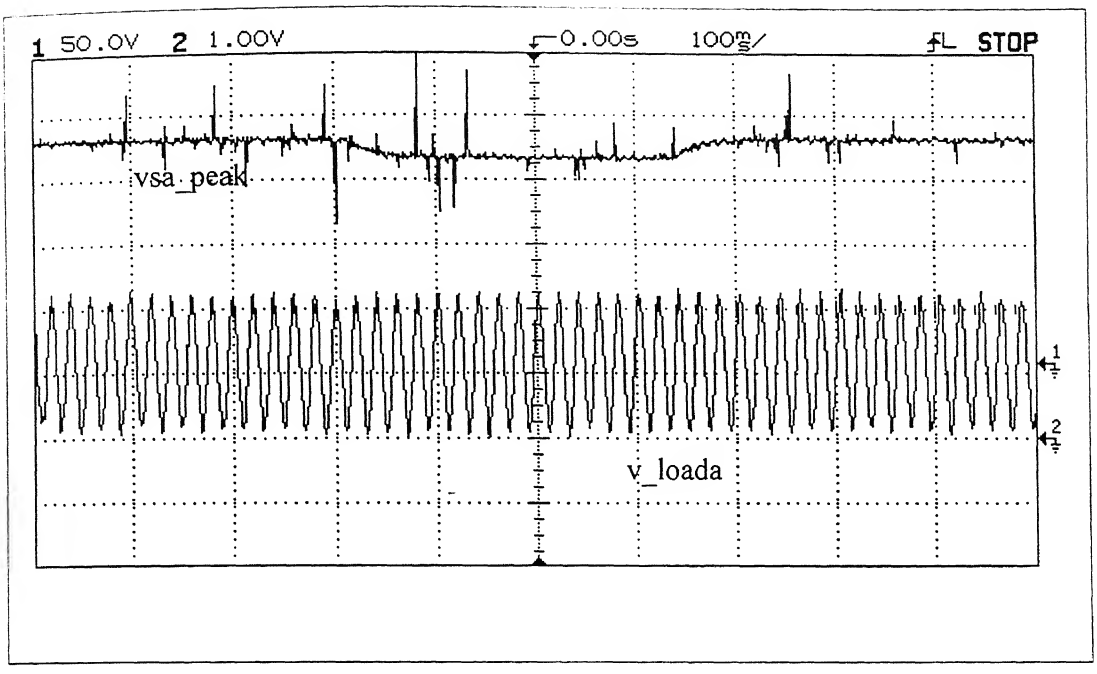

Fig. 4.23a Experimental result of peak of supply voltage and load voltage of phase-A
X axis: 100 ms/div, Y axis: 50 V/div for v_loada, 10.48 V/div for Vsa_peak,

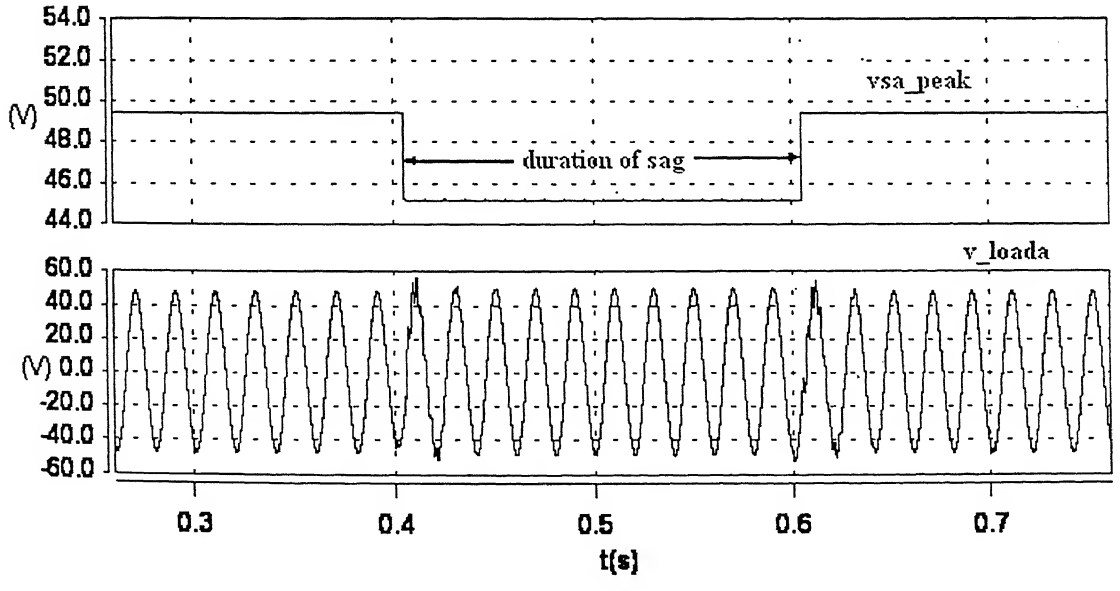

Fig. 4.23b Simulated result of peak of supply voltage and load voltage of phase-A

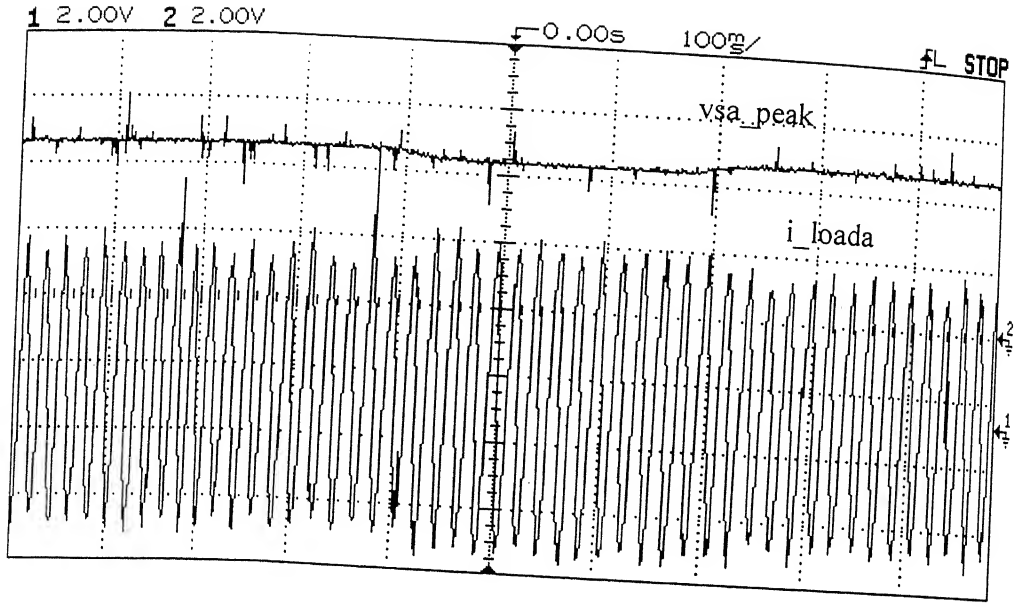

Fig. 4.24a Experimental result of peak of supply voltage and supply current of phase-A
X axis: 100 ms/div, Y axis: 20.96 V/div for Vsa_peak, 2 A/div for i_loada

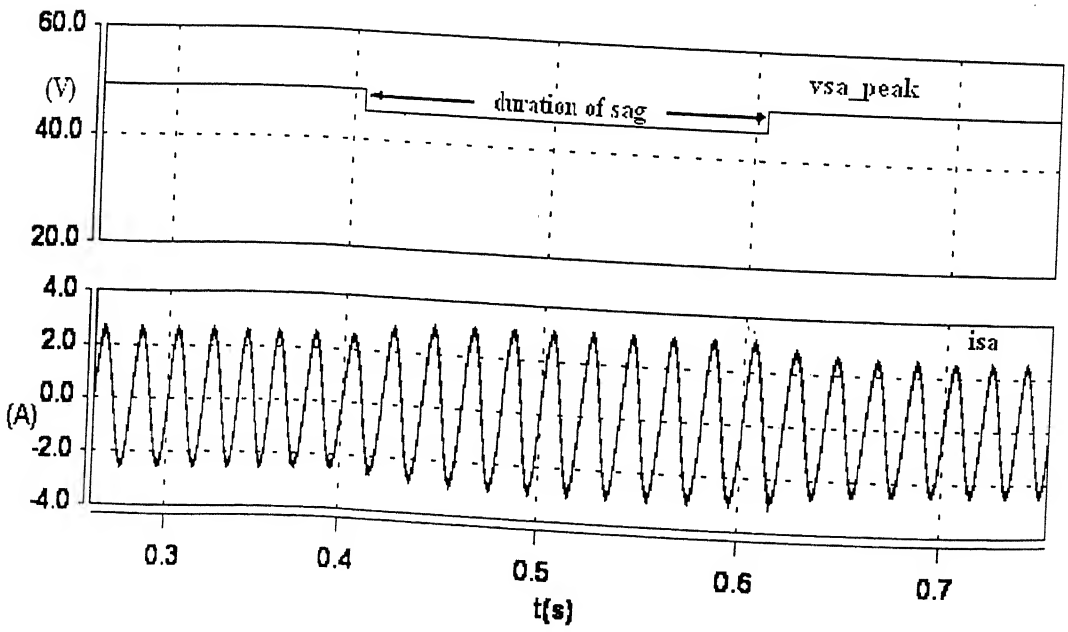

Fig. 4.24b Simulated result of peak of supply voltage and supply current phase-A

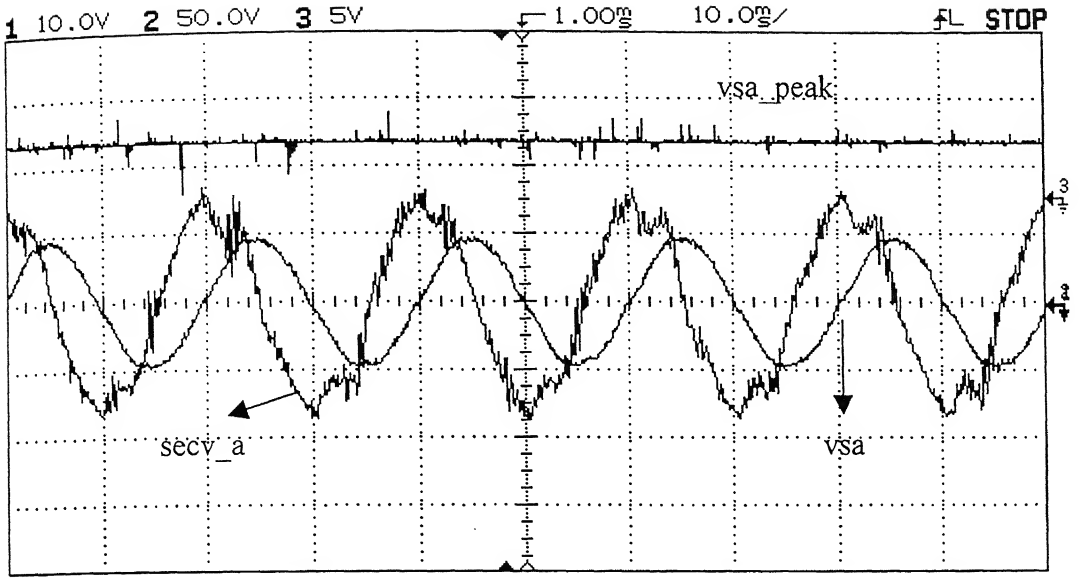

Fig. 4.25a Experimental result of peak of supply voltage and injected voltage and supply voltage of phase-A, X axis: 10 ms/div, Y axis: 10 V/div for secv_a, 50 V/div for vsa, 52.4 V/div for Vsa_peak

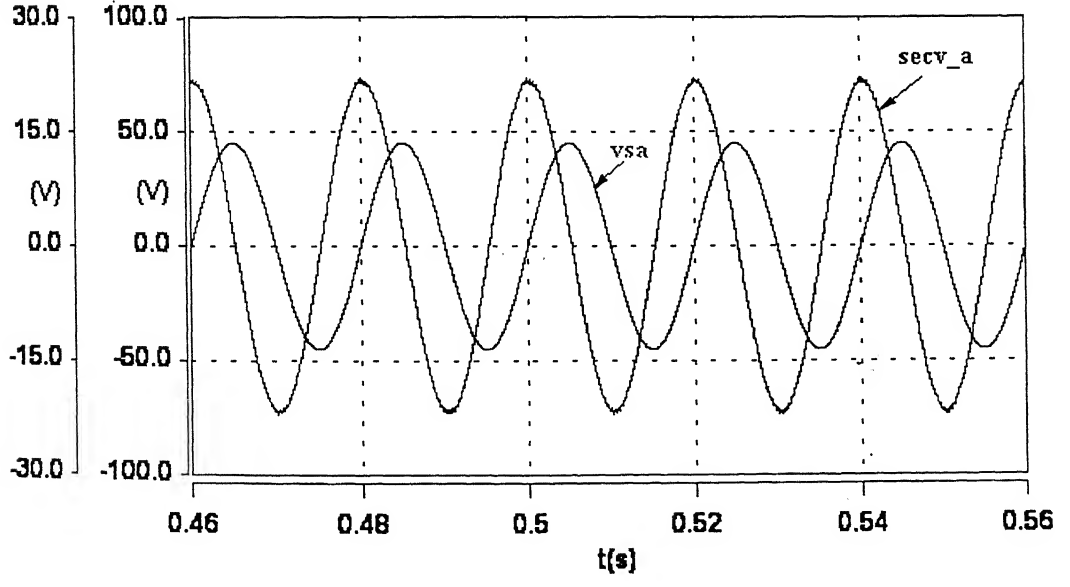

Fig. 4.25b Simulated result of injected voltage and supply voltage of phase-A

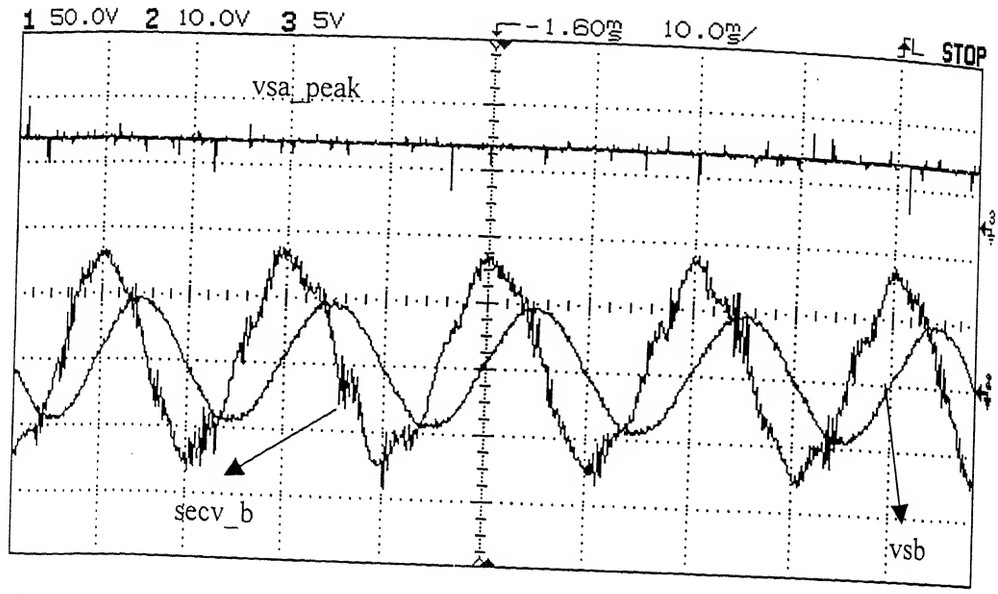

Fig. 4.26a Experimental result of peak of supply voltage and injected voltage and supply voltage of phase-B, X axis: 10 ms/div, Y axis: 50 V/div for vsb, 10 V/div for secv_b, 52.4 V/div for Vsa_peak

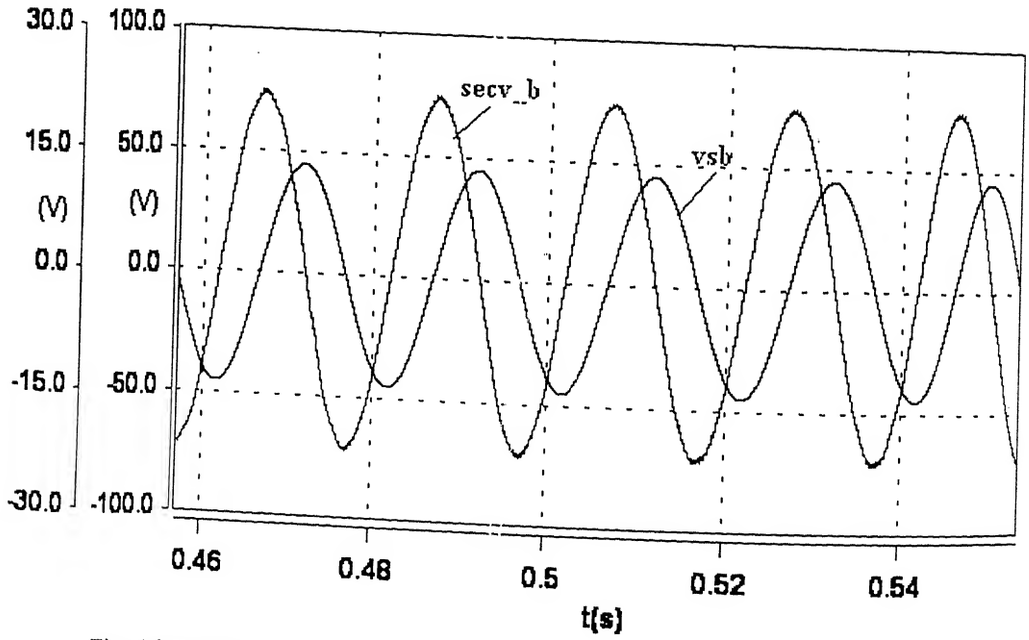

Fig. 4.26b Simulated result of injected voltage and supply voltage of phase-B

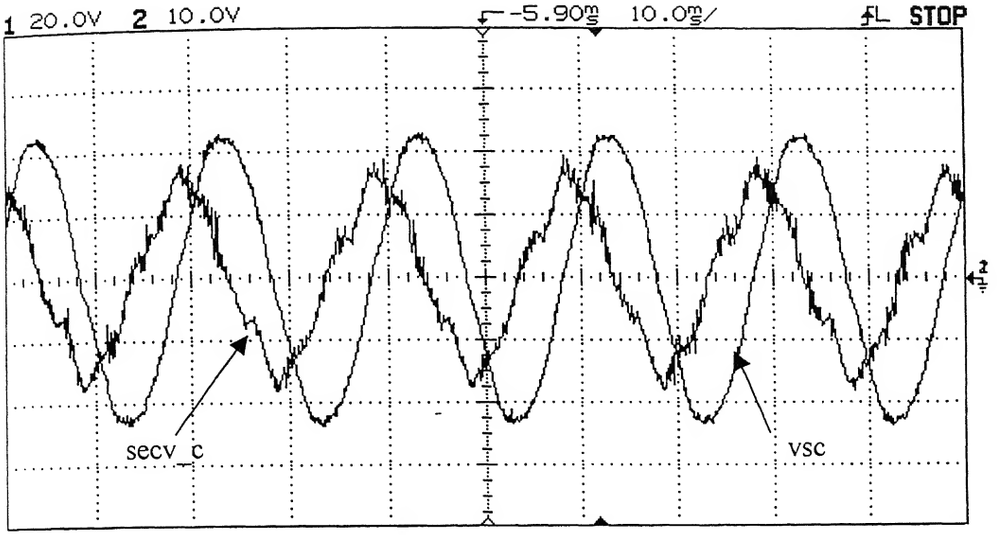

Fig. 4.27a Experimental result of injected voltage and supply voltage of phase-C, X axis: 10ms/div, Y axis: 20 V/div for vsc, 10 V/div for secv_c

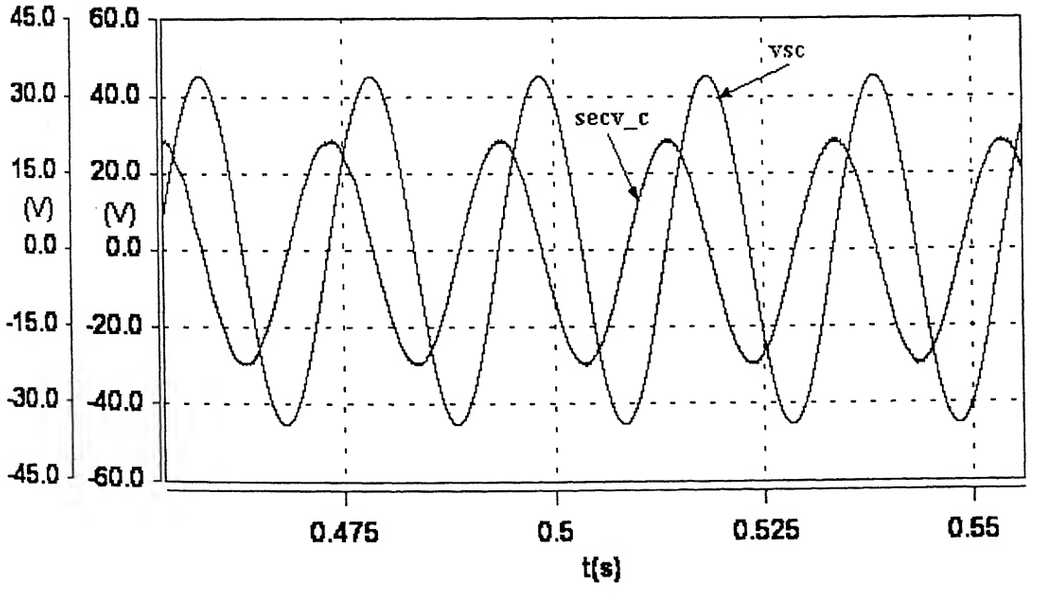

Fig. 4.27b Simulated result of peak of supply voltage and injected voltage and supply voltage of phase-C

4.7 Some Studies on UPQC-P

So far in Chapters 3 and 4 the control strategy and performance of UPQC-Q has been investigated. In this section the performance of UPQC-P is studied. The power circuit of UPQC-P is not different from UPQC-Q. However, the series inverter injects voltage in phase with the supply voltage in UPQC-P. Therefore the series inverter consumes active power from the common dc link of the UPQC, and it does not share reactive VA of the load with the SLCVC unlike UPQC-Q. However, with a suitable control scheme, UPQC-P can mitigate unbalanced supply voltage sag, which UPQC-Q cannot do.

4.8 Phasor Diagram and VA Rating of UPQC-P

The phasor diagram of Fig. 4.28 explains the operation of UPQC-P for the fundamental frequency. When the system voltage and current are in phase due to the action of the shunt compensator, the series converter handles purely active power. As seen from Fig. 4.28, the shunt compensator current increases when there is a supply voltage sag, as the series inverter consumes active power through the shunt compensator. When the supply sag is created, the series inverter of the UPQC should compensate for the fall in voltage to maintain the load voltage to its specified value. The injected voltage being in-phase with the supply voltage, the supply current and injected voltages are also in-phase with each other. Hence, the series inverter handles only active power. The series inverter delivers this additional active power by drawing the same from the dc link of the UPQC. Therefore, it acts as an active load to the shunt converter (SLCVC). As seen from the phasor diagram, I_{c2} has an additional active and same reactive component as I_{c1}.

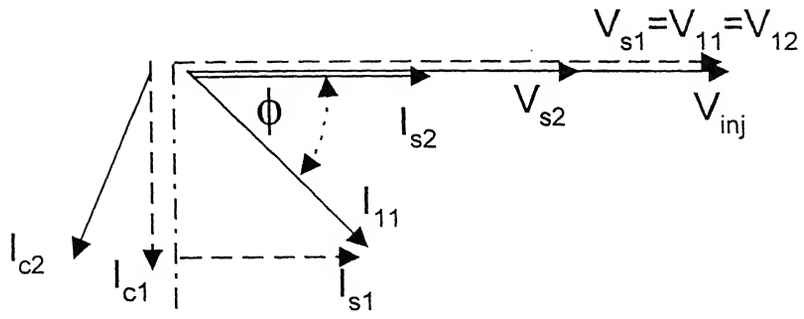

Fig. 4.28 Phasor diagram of UPQC-P

The loading calculation of UPQC-P has been carried out on the basis of linear load. From phasor diagram of Fig. 4.28, it can be found that for each phase

$V_{l1} = V_{l2} = V_{s1} = Constant = 1$ p.u. (4.1)

If load current is assumed to be $I_l = I_{l1} = I_{l2} = 1$ p.u, (4.2)

with fundamental p.f. = cosϕ, active power demand in the load remains the same,

i.e. $V_s I_s = V_l I_l \cos\phi$ = Constant (4.3)

In case of sag when $V_{s2} < V_{s1}$, where x denotes the p.u. sag,

$V_{s2} = (1-x)\ V_{s1} = (1-x)$ p.u. (4.4)

Now, to maintain constant active power

$V_{s1} I_{s1} = V_{s2} I_{s2}$ (4.5)

Or, $I_{s2} = (1.I_l \cos\phi)/(1-x) = \cos\phi/(1-x)$ p.u. (4.6)

$\therefore$ Series VA Rating = $V_{inj}.\ I_{s2} = (x.\cos\phi)/(1-x)$ p.u. (4.7)

$$I_{c2} = \sqrt{I_{l1}^2 + I_{s2}^2 - 2I_{l1}I_{s2}\cos\phi}$$

$$= \frac{\sqrt{(1-x)^2 + \cos^2\phi\{1-2(1-x)\}}}{(1-x)} \text{ p.u.} \quad (4.8)$$

$\therefore$ Shunt VA Rating

$$= \frac{1}{(1-x)}\sqrt{(1-x)^2 + \cos^2\phi\{1-2(1-x)\}} + \frac{(1-x)^2 + \cos^2\phi\{1-2(1-x)\}}{(1-x)^2} Z_{SLC} \text{ p.u.} \quad (4.9)$$

Adding (4.7) and (4.9), the total VA rating of the UPQC-P is found to be

$$\text{VA - P} = (x\cos\phi)/(1-x) + \frac{1}{(1-x)}\sqrt{(1-x)^2 + \cos^2\phi\{1-2(1-x)\}} + \frac{(1-x)^2 + \cos^2\phi\{1-2(1-x)\}}{(1-x)^2} Z_{SLC} \text{ p.u.} \quad (4.10)$$

Graphically these series, shunt and combined VA loadings are presented in Figs. 4.29, 4.30 and 4.31.

It is observed from the graphs that the series VA loading (Fig. 4.29) increases as percentage sag increases. Also it is obvious that as series inverter consumes active power, the rating of the inverter also goes high with the load power factor, as the inverter has to allow the active component of load current through it. The shunt VA loading (Fig. 4.30) variations are not very significant in the event of a voltage sag for low power factors, as the active part of current will be significantly less compared to the reactive part of load current. But for higher power factor (say p.f. 0.9), the active component of converter current is comparable with the reactive current of load and the loading increases appreciably while compensating a voltage sag.

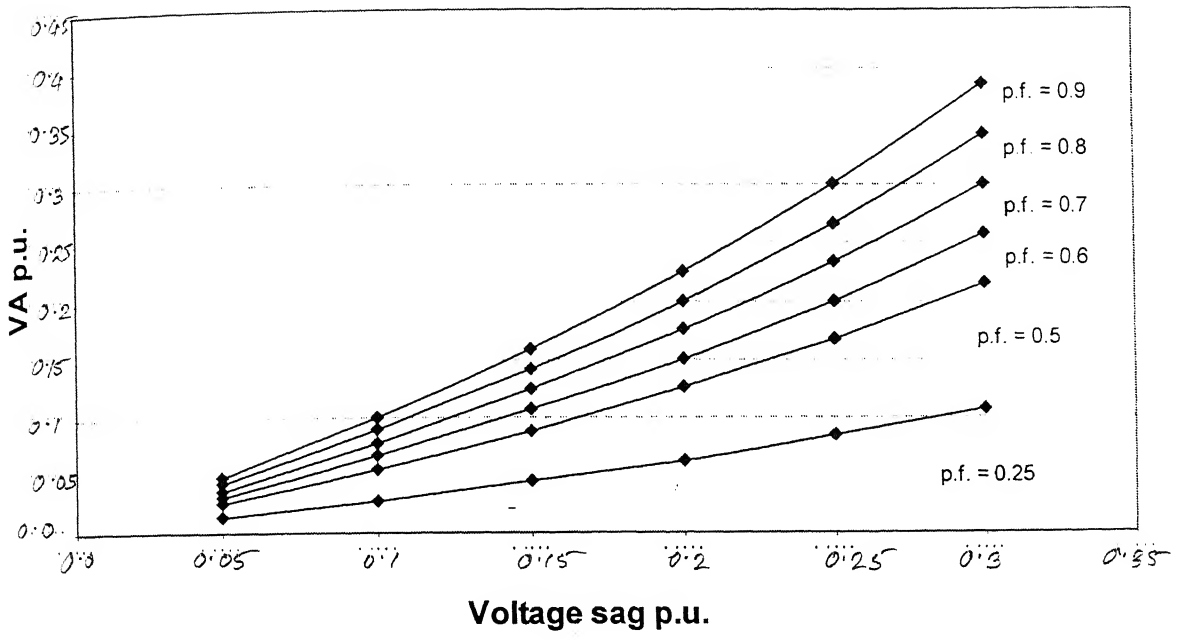

Fig. 4.29 Per unit VA loading of UPQC-P series inverter against p.u. voltage sag to be mitigated for various load power factor

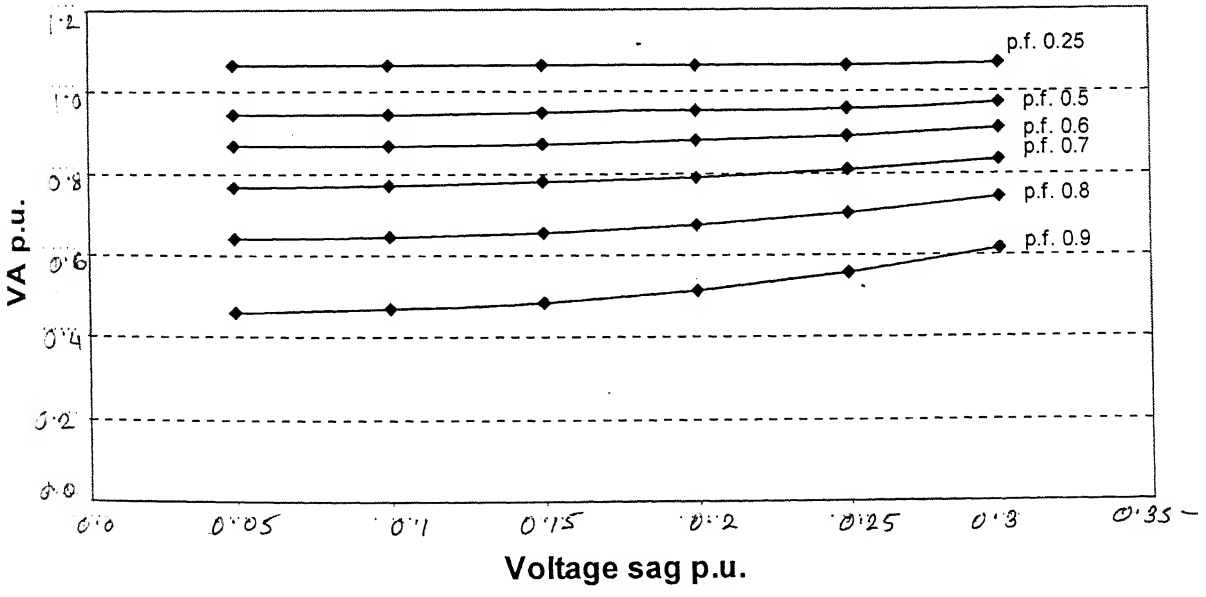

Fig. 4.30 Per unit VA loading of UPQC-P shunt inverter against p.u. voltage sag to be mitigated for various load power factor

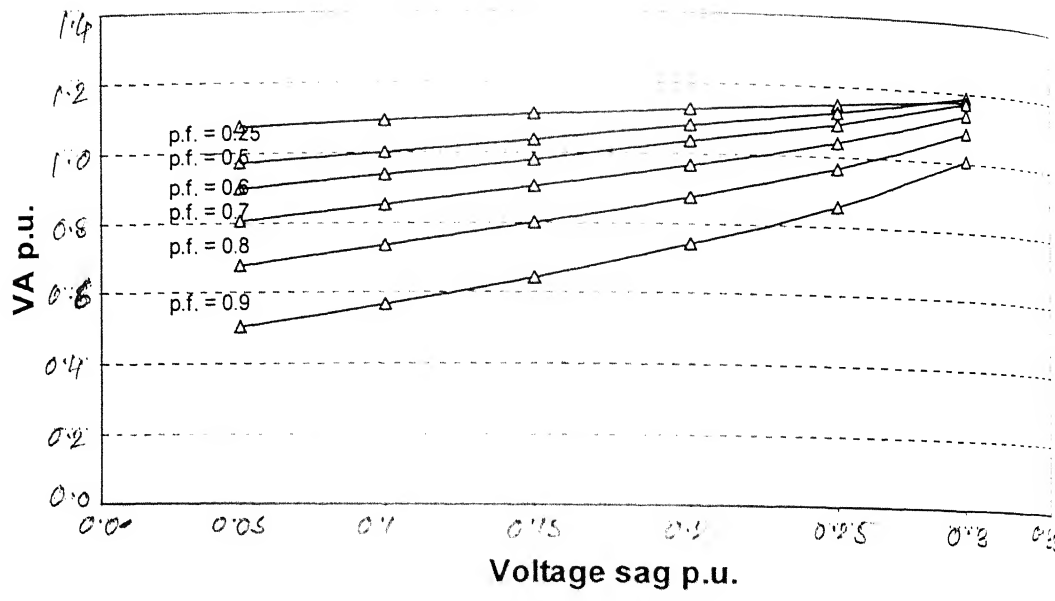

Fig. 4.31Total per unit VA loading of UPQC-P against p.u. voltage sag to be mitigated for various load power factor

4.9 Control Implementation

UPQC-P is used for compensation of unbalanced supply voltage. The control of the system is based on abc-dqo analysis. In steady state and balanced supply voltage condition, d component voltage will be = 396.7 V for 230V (rms) per phase supply voltage, and q and o component will be zero. If there is a balanced supply voltage sag, the d component of voltage will deviate from the reference voltage, but q and o component will remain zero. In case of an unbalanced supply voltage sag, q and o component of voltages will be ac quantities and d component voltage will contain both ac and dc components. As all d-q-o references are known, the difference is expected to be nullified by the series inverter. The reference signals for phase A, B and C are shown in Fig. 4.32. Closed-loop PI controllers are used for compensation.

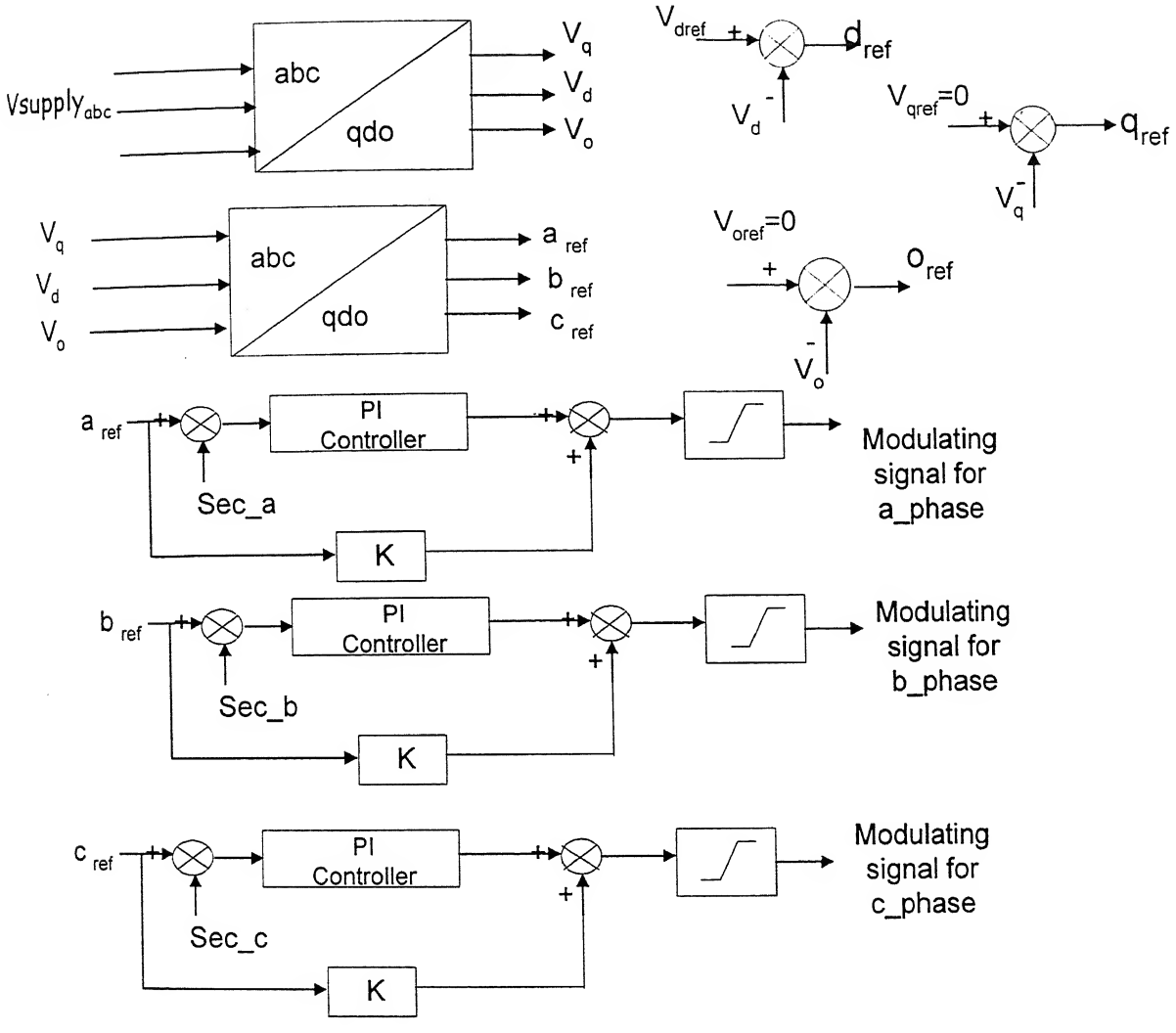

Fig. 4.32 Control block for voltage unbalance compensation

4.10 Simulation Results

The details of power and control circuits of UPQC-P have been simulated in SABER and the simulation results verify the effectiveness of the control scheme.

Figs. 4.33 to 4.35 show the performance of UPQC-P when there is a balanced supply voltage sag of 20%. Fig. 4.33 shows that even in case of supply voltage sag, the supply current remains in phase with its respective phase voltage.

Fig. 4.34 shows the load voltage profile and supply voltage profile. At t = 0.1 sec, a 20% sag is created and supply voltage peak reduces to 260 V. But the load voltage is seen to maintain its profile, with an instantanesous undershoot at the instant of occurrence of sag around 14%, which cannot be avoided. When the sag is recovered at t= 0.25 sec, there is instantaneous overshoot of 15%. Fig. 4.35 shows the changes in d-q-o components when the sag occurs. The d component of voltage reduces by 77 V, while q- and o- component of voltages remain zero.

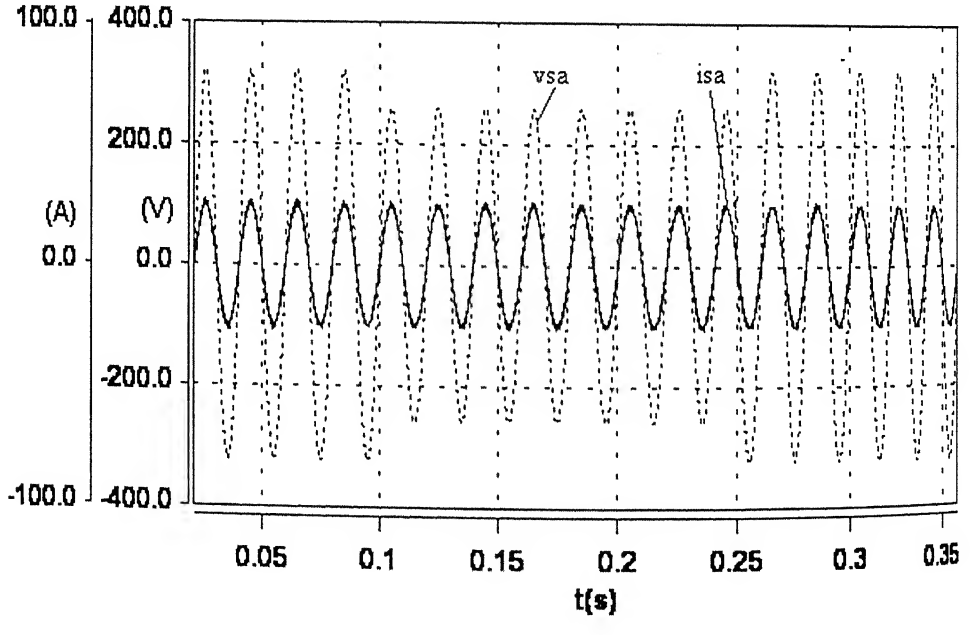

Fig. 4.33 Supply voltage and current of phase A under normal and 20% sag condition

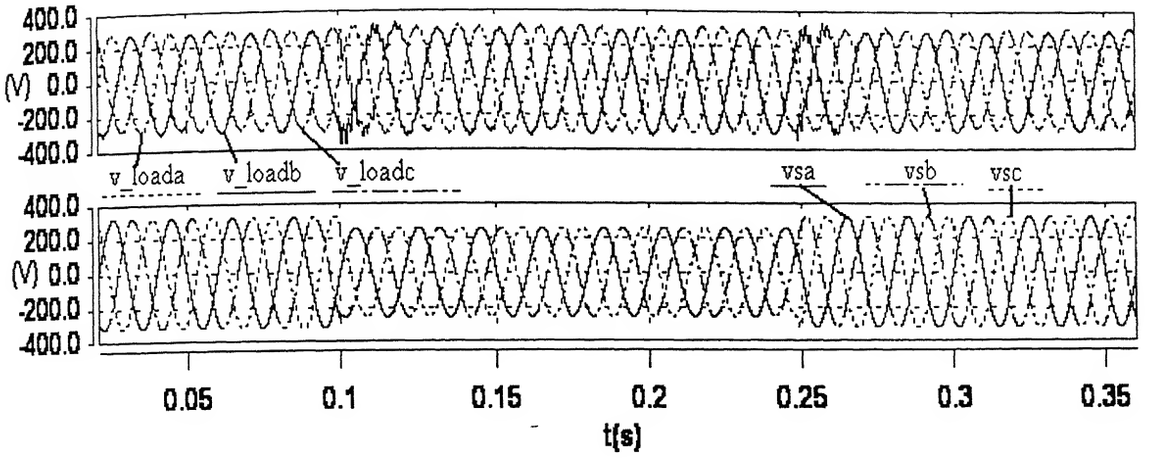

Fig. 4.34 Load voltage and supply voltage profile under normal and 20% balanced sag condition

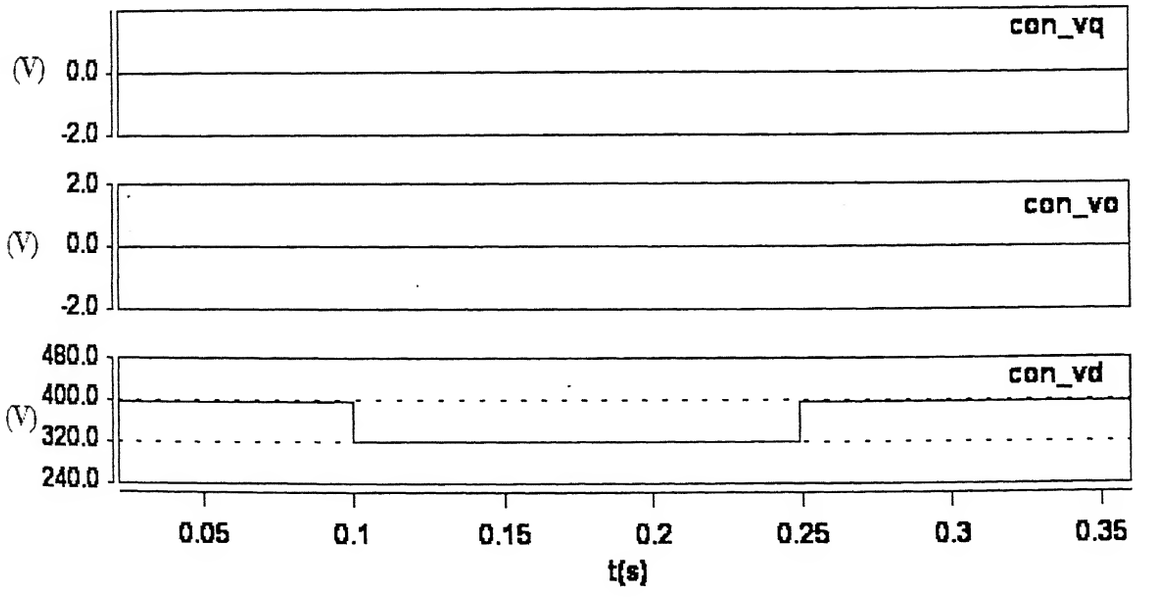

Fig. 4.35 d- q-o component of voltage under balanced sag condition

Figs. 4.36 to 4.42 present the performance of UPQC-P for unbalanced voltage sag mitigation. In Fig. 4.36 it is found that at t = 0.1 sec, the peak of three phase voltages become 300 V, 275 V and 250 V in phases A B and C respectively. But the lower trace of load voltages are balanced and are maintained to the desired value of 230 V(rms) (325 V peak). From Fig. 4.37, it is found that when a supply voltage sag occurs, q-component voltage becomes ac peak to peak of 35 V with frequency 100 Hz, o-component voltage becomes ac peak to peak of 50 V with frequency 100 Hz. The d-component voltage is seen to be reduced by 60 V with a superimposed voltage ripple of 35 V (peak to peak, with frequency 100 Hz). Figs. 4.38 to 4.40 show each supply phase voltage and current. It is seen that even during sag, nearly unity input power factor is maintained.

The steady state load current, the supply current and SLCVC current of phase A are shown in Fig. 4.41.

The harmonic spectra of load voltage is shown in Fig. 4.42. It is found that after series injection of voltage by UPQC, the load voltage harmonic spectra remain within IEEE specified limit of 5%. Thus the simulation results show satisfactory performance of UPQC-P.

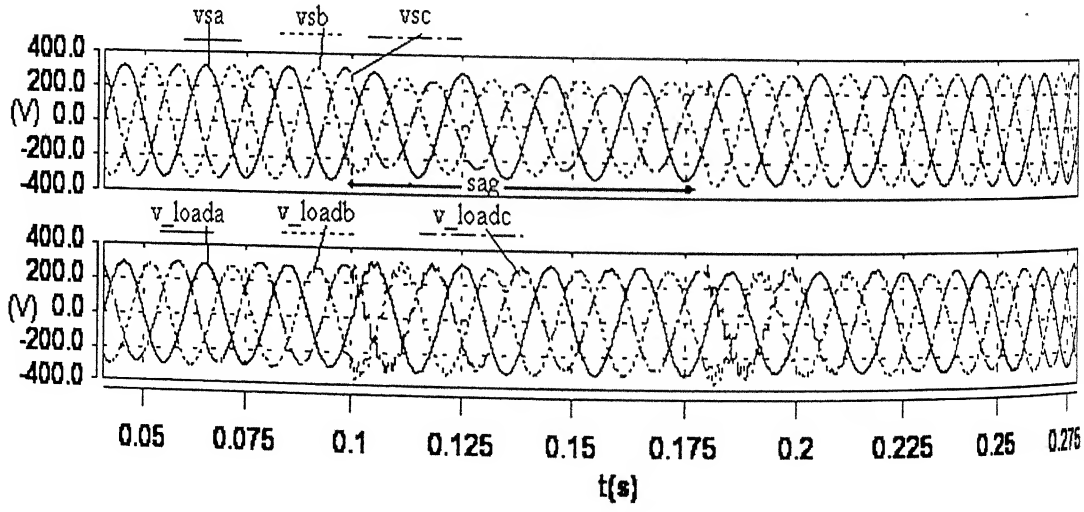

Fig. 4.36 Load voltage and supply voltage profile under normal and unbalanced sag condition

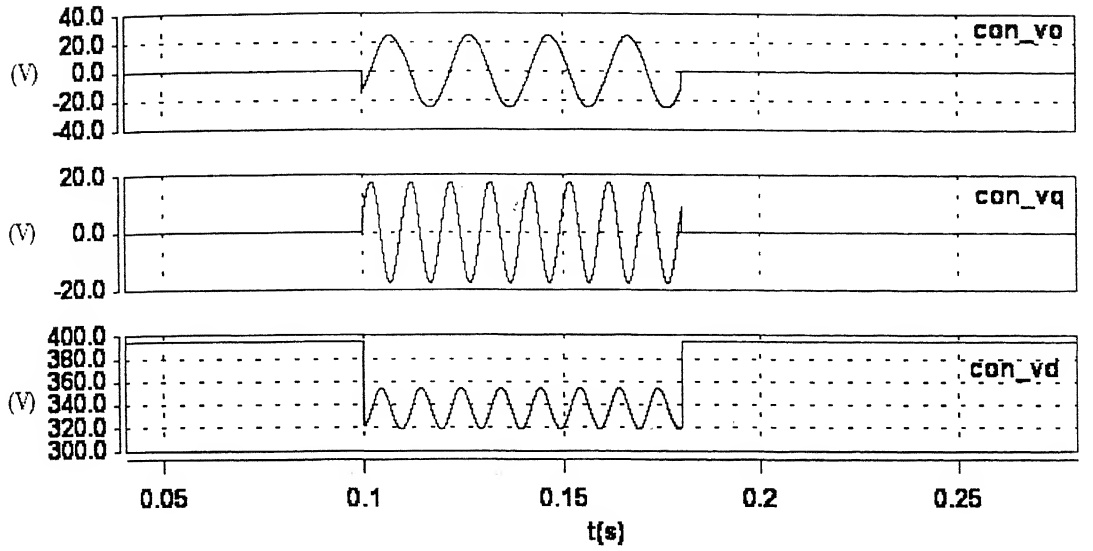

Fig. 4.37 d- q-o component of voltage under balanced sag condition

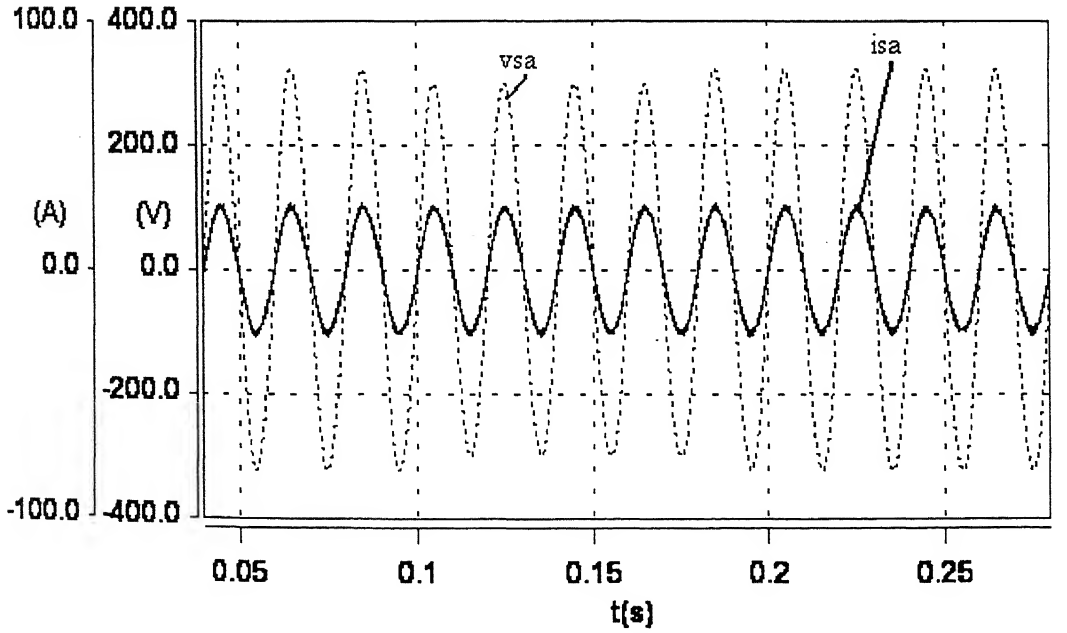

Fig. 4.38 Supply voltage and current of phase A under normal and unbalanced sag condition

4.11 Conclusion

The present chapter investigates the performance of three phase UPQC for non-linear load. The UPQC-Q is also implemented in the laboratory in a small power level, and the simulation and experimental results are compared to justify the control philosophy. The hybrid implementation of UPQC-Q with a PC-based control results in a modular implementation and a small sampling time of 168 μs.

UPQC-Q has the advantage of VAR sharing between the two compensators. The series compensator, while injecting voltage to mitigate the supply voltage sag, shares a part of VAR of the load and does not consume any active power.

The second part of the chapter reports the study of UPQC-P, where a suitable control strategy has been proposed. The series inverter control scheme is based on d-q-o component analysis. UPQC-P can mitigate the supply voltage-unbalancing problem also besides voltage sag. The effectiveness of the control scheme is verified through extensive simulation in SABER.

Chapter 5

A High Power Parallel Converter Topology for Load Harmonic and Reactive Power Compensation

5.1 Introduction

With rapid progress in semiconductor devices technology, active solution to VAR compensation and harmonic elimination of loads are preferred to passive filter solutions due to availability of fast acting switching devices having moderate power rating. But, long tail current associated with the device characteristics prohibits high switching frequency operation at high power. Also at high power, efficiency of Active Power Filters (APF) is less due to significant switching loss. Therefore, current quality control in high power application faces difficulty. To attend this problem, a new technique by combining high power low frequency devices and low power high frequency devices has been reported to extract superior performance in VAR compensation [70, 71]. A high power converter (main converter), which consists of high power low switching frequency devices, is operated at low frequency to deliver the VAR requirement of the load. Another converter (auxiliary converter), which consists of low power high frequency devices is operated in parallel to it. The auxiliary converter eliminates the harmonics produced by the main converter and that of the load such that the utility current THD is less than the specified value in IEEE-519 standard for a particular level of current. Additionally, the power rating of the auxiliary converter is low as it does not handle the reactive load current. The main converter is a voltage source inverter (VSI), which is controlled in

selective harmonic elimination technique such that, a few lower order harmonics are eliminated with moderate switching frequency of about 400 Hz.

To further lower the switching frequency of the main converter for high power applications, a new combination of power circuit topology has been investigated along with suitable control technique. Attempts have been focused on the effectiveness of a three level Neutral Point Clamped (NPC) inverter [72, 73], which can be rated for high power (main converter), as one of the parallel converters with a dedicated task of VAR compensation of load at fundamental power frequency. Two types of parallel configurations have been investigated and compared for sharing of VAR support and load current harmonic elimination, so that a suitable combination can be chosen to maximize the efficiency of the parallel load compensation scheme.

While the present topology aims at the compensation of load VAR and harmonics by a shunt connected system, the supply voltage sag can be compensated by an independent series converter with a self sustained dc link. The injected voltage will remain in quadrature advance with the supply voltage such that the series compensator would not consume active power, except to sustain the dc link voltage for the converter losses. Thus, the voltage sag compensator can be mutually independent of the current controller. The topology and control for the shunt controller scheme being new, the present chapter will address in detail the issues involved with shunt converter only.

To show the usefulness of the proposed control scheme, an extensive simulation study has been carried out using SABER simulator.

5.2 Power Circuit Configuration

A three phase three wire star connected utility is considered. The combined Active Power Filter is connected in parallel to the load.

The main converter is either a neutral point clamped (NPC) three level inverter (Fig. 5.1), or, a six-step voltage source inverter (VSI) (Fig. 5.3), with high power low frequency devices (like GTO). By keeping the switching frequency to fundamental only, the switching loss is minimized and the full utilization of the current carrying capability of switching devices is realized. Thus the main converter can carry high reactive power demand of the load.

The auxiliary converter consists of low power high frequency devices (like IGBT), controlled by current controlled modulation technique. It eliminates the main converter current harmonics and the load current harmonics from flowing to the utility current by high switching frequency operation. The two converters share the same dc link capacitor leading to a compact structure.

To avoid circulating currents between the two converters, the auxiliary converter is connected in parallel to the load as well as main converter with an isolation transformer. This prevents the circulating reactive current between the two converters even though they share the common dc link.

The effects of both linear and non-linear loads have been studied. The non-linear load under study is a phase controlled rectifier, which simultaneously produces VAR and large current harmonics.

5.2.1 Parallel NPC converter configuration

Fig. 5.1 shows the power circuit configuration with a NPC three level inverter as the main power converter of the proposed parallel active power filter scheme, which will be termed as Neutral Point Clamped converter based Active Power Filter (NPC - APF).
With the increase in the number of levels of voltage in the multilevel converter, the converter-produced harmonics would have reduced, but the number of components of the converter would have increased [31], and control would have been more complex. In the present scheme, the main converter harmonics are taken care of by a low power high switching frequency auxiliary converter and the NPC converter is operated at fundamental power frequency for load reactive power compensation to reduce control complexity.

As found from Fig. 5.1, half of each phase leg is split into two series connected switches and mid-point of each pair is connected by diodes (like $\mathbf{D_{f1}}$ and $\mathbf{D_{f4}}$ in phase A) to the midpoint **N** of the two capacitors.

Here the voltages across the switches are only half of the dc link voltage. Fig. 5.2a shows the NPC converter output voltage for phase A. When the voltage is positive, switches **1, 1m** conduct, and when the voltage is negative, **4, 4m** conduct. When the phase

voltage is connected to the neutral point N (i.e., zero voltage), switches **1m, 4m** conduct [48].

The present NPC converter topology leads to doubling the number of switches in addition to two extra clamping diodes. However, doubling the number of switches with same voltage rating makes the dc voltage rating to double, and this increases power handling capability of the converter.

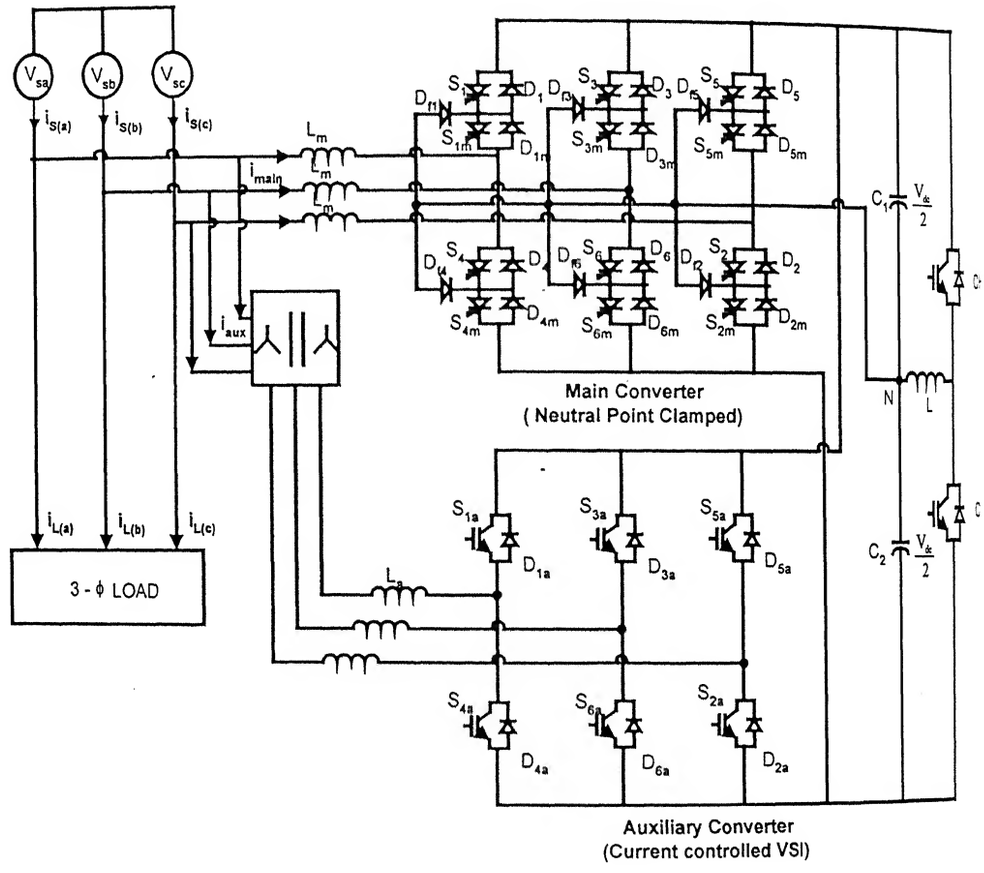

Fig. 5.1 Power circuit configuration of NPC - APF

It is essential to ensure that the two capacitors are charged to same voltage because unequal voltages will generate even harmonics. A simple chopper circuit (with two switches and an inductor of 10 mH) has been used to maintain the charge balanced between two capacitors (shown in Fig. 5.1). The filter inductance (L_m) for the main converter is 10 mH and that for the auxiliary converter (L_a) is 4 mH. Each dc link capacitor (C_1 and C_2) is 1000 μF.

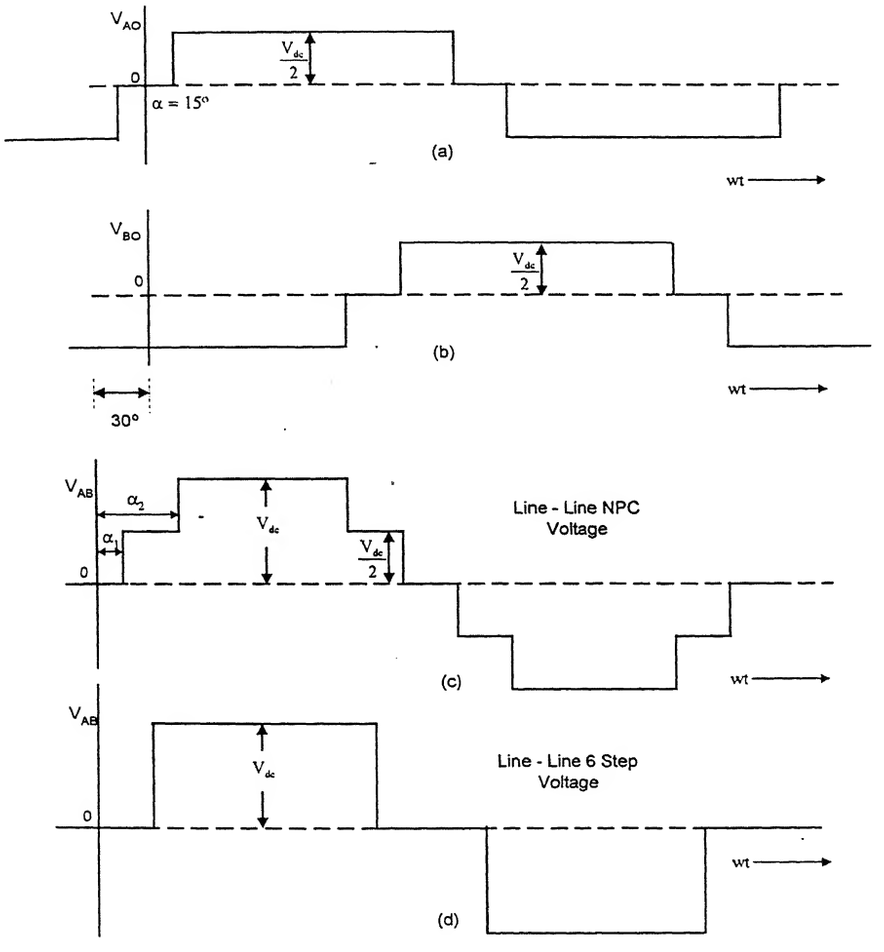

Fig. 5.2 Typical phase and line voltage of NPC converter and 6 - step converter.

a) Phase to neutral voltage of NPC converter (V_{AN})

b) Phase to neutral voltage of NPC converter (V_{BN})

c) Line – Line voltage of NPC converter (V_{AB})

5.3 Control Strategy

The per phase equivalent circuit of main converter for fundamental frequency is shown in Fig. 5.4. This equivalent circuit is same for NPC-APF and 6-step-APF, as only fundamental components are considered.

Since the main converter is responsible to supply the fundamental VAR requirement of the load, the main converter current is compared with the fundamental reactive load current to generate a reactive current error.

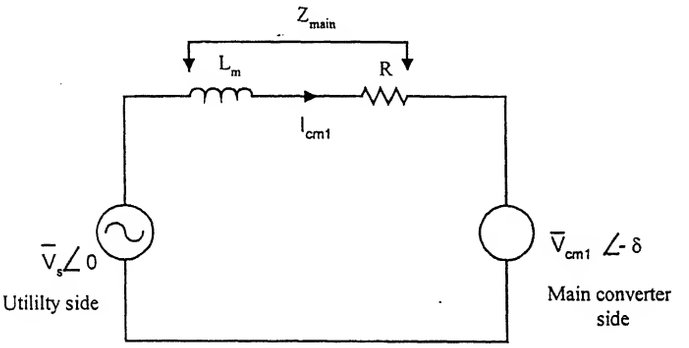

Fig. 5.4 Per phase equivalent circuit of the main converter with fundamental frequency voltage and current

The reactive current error is processed through a PI controller to control the voltage delay angle δ of the main converter for indirect current control. The change of δ leads to a change of active power flow between the utility and the main converter. Thus, the dc link voltage undergoes variation with change of δ. Since, V_{cm1} (converter fundamental voltage) is a function of V_{dc}, δ variation leads to change of V_{cm1}.

Hence, the main converter current varies according to the following equation.

$$I_{cm1} = \left(\frac{V_s - V_{cm1} \angle -\delta}{Z_{main}} \right) \quad \ldots \quad (5.1)$$

where, V_s is the supply voltage, Z_{main} is the impedance of the inductor (L_m) connecting the main converter to the supply, and I_{cm1} is the fundamental rms current of the main converter. With the information of δ, the modulating signals are adjusted to trigger the main converter switches.

5.3.1 Estimation of δ and reference current

The complete system control block diagrams for both topologies (NPC-APF and 6-Step-APF) have been given in Fig. 5.5 and Fig. 5.6. It is desirable that the utility should supply only the active component of load current and the loss component of the converters at unity power factor. Therefore, the supply current should be always in phase with respective phase voltage. In ideal case, angle δ is supposed to be zero, as the main converter current caters only the load reactive current, which is at quadrature with the supply voltage. However, because of the converter losses, the capacitor voltage tends to fall and requires small amount of active current from the supply to maintain the charge. So the angle δ acts as a measure of converter losses and a control signal proportional to δ is added with the active component of load current ($|i_{Lact}|$) to determine the reference magnitude of the source current. This amplitude, multiplied by a sin-template (in phase with respective utility phase voltage) gives the reference utility current (i_s*) for the respective phase.

For non-linear loads, a band pass filter is used to extract the fundamental component of load current and its active and reactive components are separated out. The reactive component of fundamental load current ($|i_{Lreact}|$) is compared with the reactive component of the main converter current ($|i_{main\_reactive}|$) and the error is processed through a PI controller. The output of the controller acts as the information δ (for indirect current control) and modulating signals of the main converter are modified accordingly.

Inverter with low impedance and fast response tends to be overloaded in case of transient situation. So, for the start-up, the auxiliary converter is initially not triggered. When the main converter current reaches a steady value and the VAR of the load is supplied locally from the main converter, the utility supplies the active component of currents and some higher order

harmonics. After the auxiliary converter is switched on, the higher order harmonic currents are supplied from the auxiliary converter and the utility supplies only the fundamental active component of current. The magnitude of the utility current reference is addition of two signal components, namely fundamental active load component of current ($|i_{Lact}|$), and a component which brings information about δ (for the loss component of the converters). This amplitude multiplied by appropriate sinusoidal template of each phase in the reference current generator produces utility current reference (i_s^*). The actual supply current (i_s) is then compared with i_s^* in a hysteresis controller and the output of the controller determines the switching of the auxiliary converter.

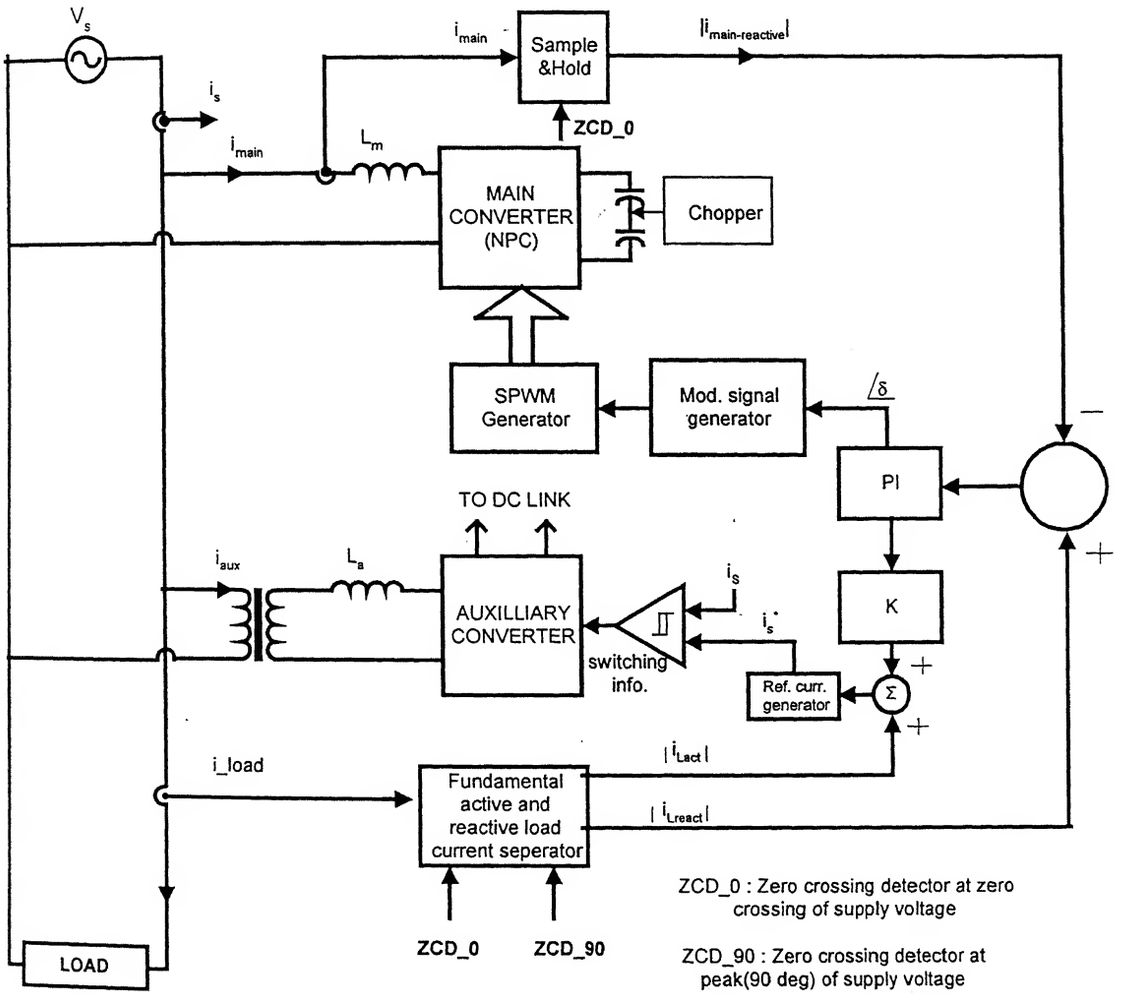

Fig. 5.5 Control block diagram of the proposed compensator scheme of NPC - APF

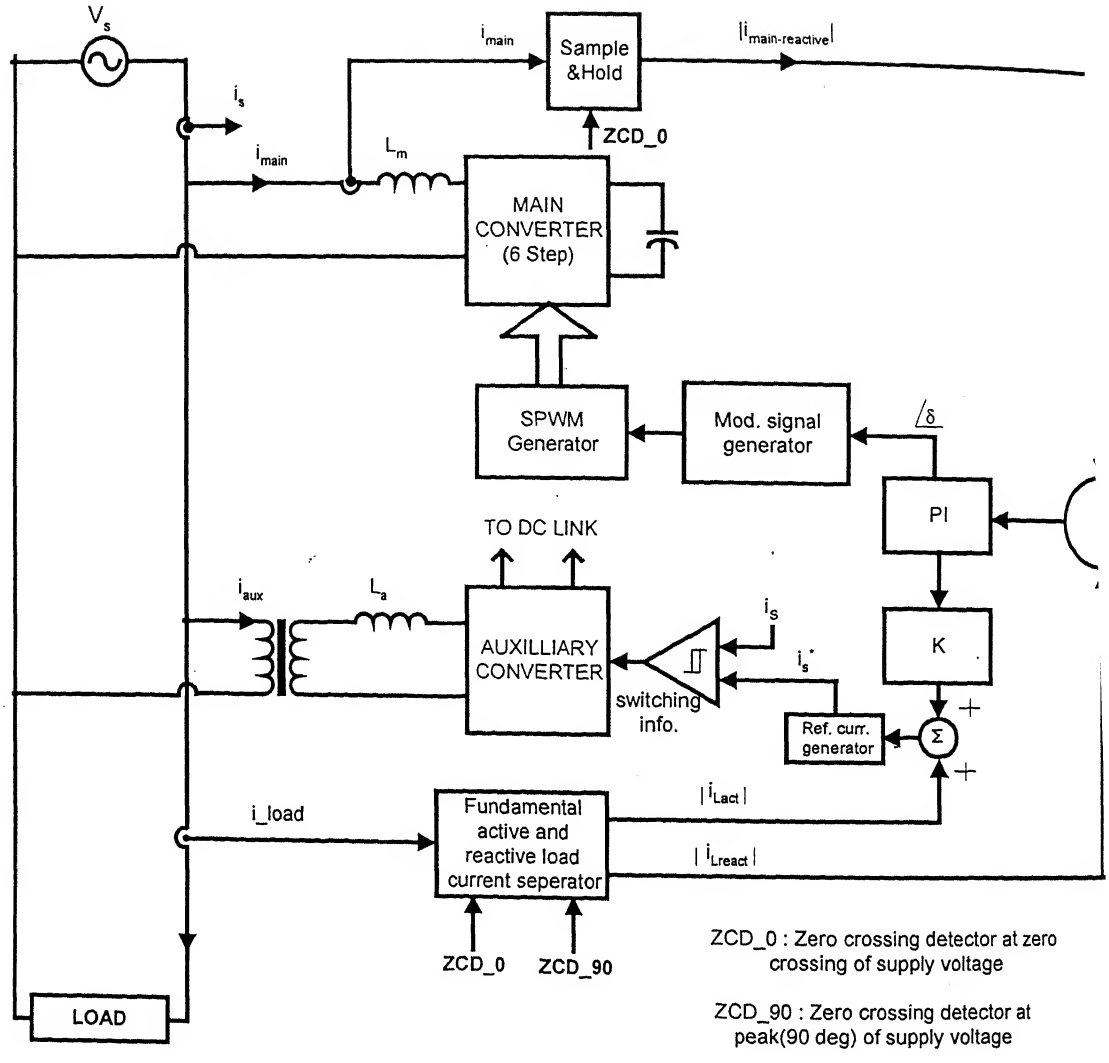

Fig. 5.6 Control block diagram for 6-Step - APF

5.3.2 Control signal for main converter (NPC Inverter and 6-step Inverter)

As seen in Figs. 5.2a, b (the phase voltage of NPC converter), if α be the firing angle, then the converter voltage would be [48, 73]

$$e_{npc} = \frac{4}{\pi n} \sum V_1 \cos n\alpha \sin n\omega t \qquad (5.2)$$

where, ω corresponds to the fundamental power frequency,

and $V_1 = 0.5V_{dc}$.

If $\alpha = 18°$, the 5^{th} harmonic will be zero,

If $\alpha = 12.85°$, the 7^{th} harmonic will be zero, etc.

Fig. 5.2a shows the typical line to line voltage of a NPC converter.

Here, the n^{th} harmonic voltage would be

$V_{Ln} = V_1 \cos(n\alpha_1) + V_2 \cos(n\alpha_2)$

As V_1 and V_2 are equal to 0.5 V_{dc}, and $\alpha_1 = (\pi/3 - \alpha_2)$

$V_{Ln} = \left[\cos n\left(\frac{\pi}{3} - \alpha_2\right) + \cos(n\alpha_2)\right]$, where α_2 can be selected to eliminate any particular harmonic, so as to reduce the total harmonic distortion. Eliminating one particular harmonic will not significantly improve the wave shape; therefore minimizing the total harmonic distortion (THD) would be desirable. It has been reported in literature [73] that to keep converter's 5^{th} and 7^{th} harmonics low, and the overall THD minimum, the converter firing angle should be $\alpha = 15°$, which has been chosen in the present investigation.

The control of six-step inverter is the conventional 180° conduction, typical line to line voltage is shown in Fig. 5.2d.

It has been found that THD in the voltage waveform of six-step inverter is around 32%, whereas the THD of the voltage waveform of the NPC converter is only 16%.

The auxiliary converter is a current controlled VSI. The difference between actual supply current and the reference utility current (obtained as mentioned in sec. 5.3.1) is processed through a hysteresis controller. The hysteresis window is selected in such a manner that the THD of the utility current remains within IEEE-519 specified limit of 5%. This limit has been

chosen considering the worst case I_{sc}/I_L ratio at PCC. The output of the controller acts as switching information to the auxiliary converter.

5.3.3 Control of dc link voltage and chopper control

In the present control scheme, the dc link voltage is not compared with a pre-specified reference. It automatically charges up or down according to the VAR requirement of the load. A chopper circuit is used to keep the two capacitors charged to equal voltage. Whenever, one capacitor overcharges with respect to the other, a circulating current flows from one capacitor to the other through an inductor of 10 mH, such that the two capacitors are brought back to equal voltage. The chopping frequency is 5 kHz.

5.4 Simulation Study

Detailed simulation studies are carried out with SABER simulator to observe the performance of the combined compensators with the proposed control law.
For the start-up process, the main converter is switched on, and after the current has reached steady state, auxiliary converter is made on.

5.4.1 Performance of 6-Step – APF for VAR compensation of linear load

Steady state performance

A three phase star connected 100 kVA linear load is considered in a 400 V three phase three wire system. Fig. 5.7 shows the nature of the supply current for linear load current of 145.8 A and 0.634 lagging power factor. When the main converter current reaches steady state, the auxiliary converter is turned on. It is found from Fig. 5.8 that with only main converter working, the supply current THD is 7.2% with 5^{th} and 7^{th} harmonics as 6.52% and

3.07% of the fundamental respectively. When the auxiliary converter is switched on to eliminate the main-converter harmonics and to restrict the supply current within a specified hysteresis band, the supply current THD falls to 4.59% as shown in Fig. 5.9. Now, the 5^{th} harmonic content reduces to less than 1%, and the next higher order harmonics are found to be 11^{th} harmonic (1.1%), 25^{th} harmonic (2.48%), and 43^{rd} harmonic (1.39%). The steady state currents of the main and auxiliary converter currents in all three phases are found to be balanced. The rms current ratio of auxiliary to main is found to be 14% (18.8/129.69 A). At this load condition, the dc link voltage is found to be 1370 V with peak to peak ripple of 3.4%.

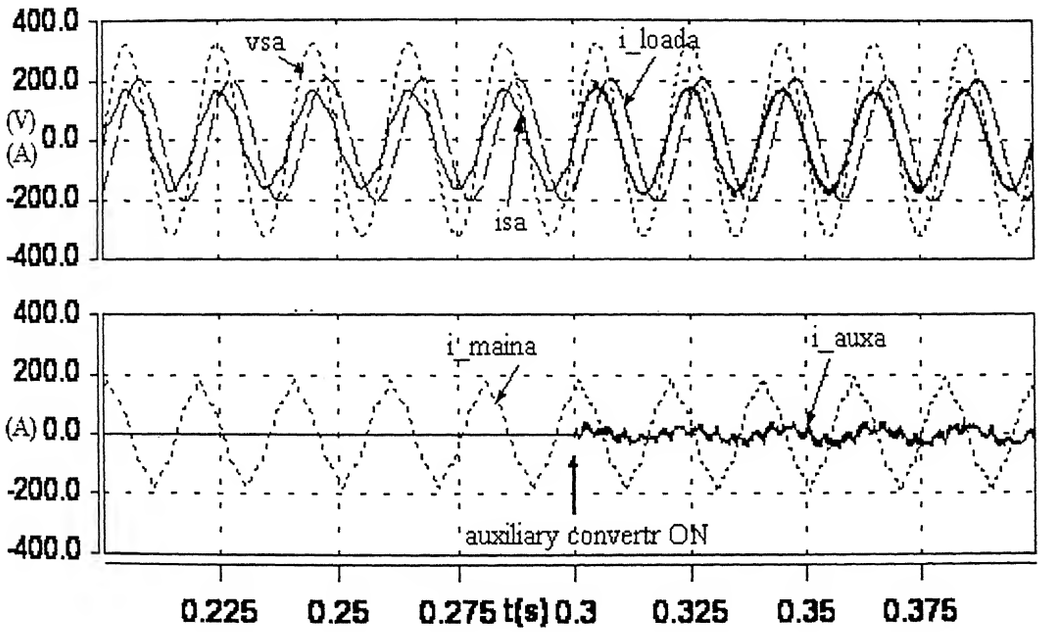

Fig. 5.7 Steady State voltage and current waveform of phase-A in 6-Step – APF

vsa = A-phase supply voltage isa = A-phase supply current

i_loada = A-phase load current

i_maina = A-phase NPC converter current

i_auxa = A-phase auxiliary current

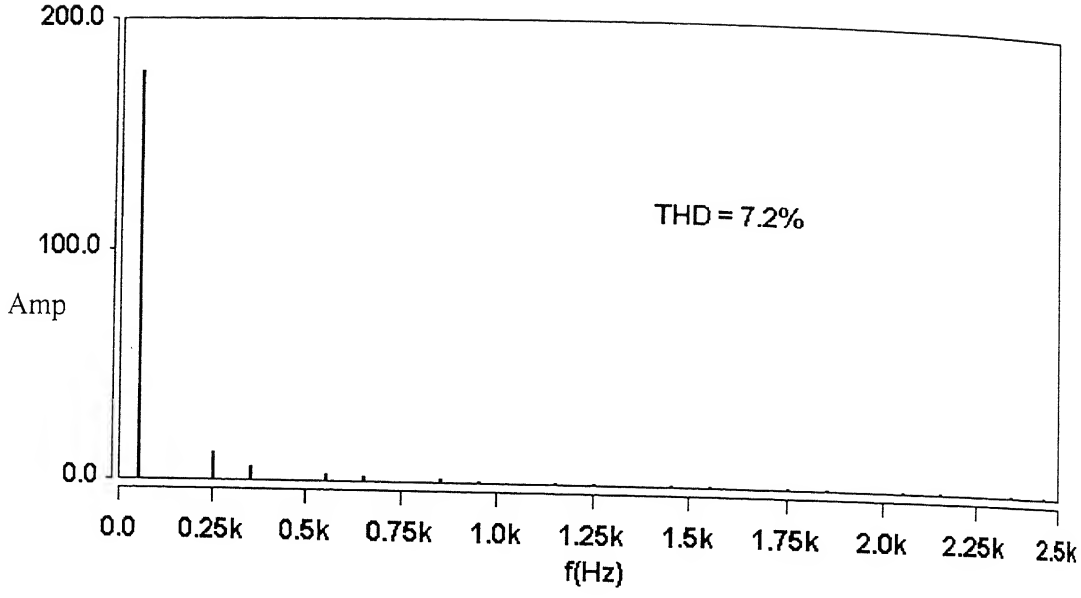

Fig. 5.8 Harmonic Spectra of the Supply Current of phase-A for 6-Step – APF scheme when auxiliary converter is not connected.

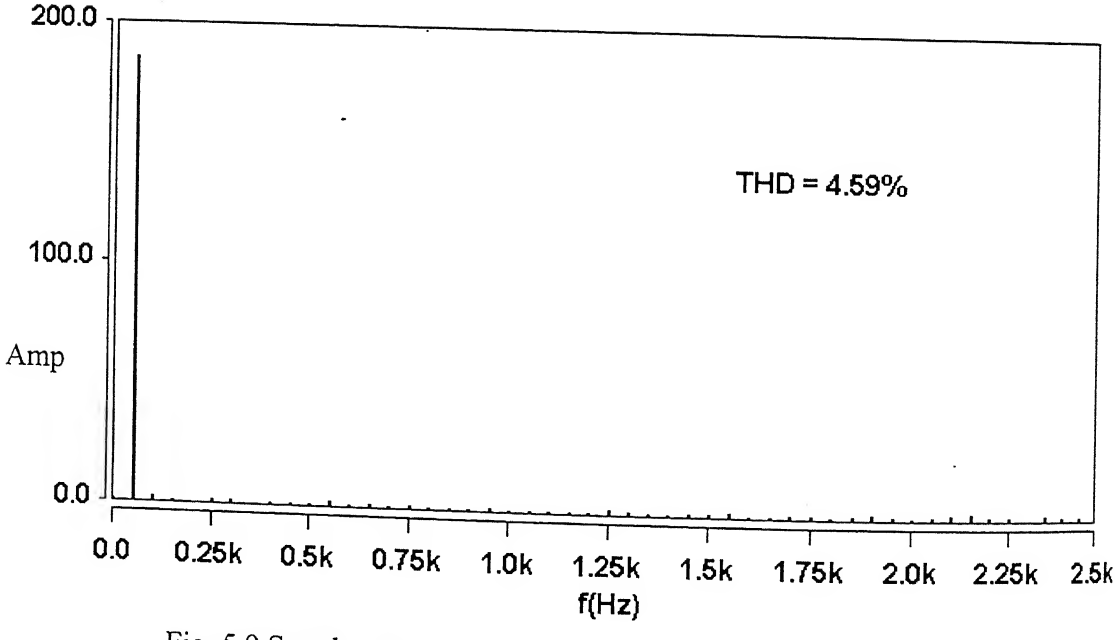

Fig. 5.9 Supply current harmonics in phase-A for 6-Step scheme when auxiliary converter is functional

Dynamic response

The dynamic response of the converter is studied when the load current is changed from 145.8 A, 0.64 p.f. lag to 170 A, 0.368 p.f. lag, and brought back to its previous value. It is observed that at all conditions, the supply current remains in phase with the supply voltage (Fig. 5.10). The effects of change in load current on the converters are observed in Figs. 5.11 and 5.12. As the response of the auxiliary converter is fast (due to direct current control), the transient change in reactive current demand of the load is taken care by the auxiliary converter. But as soon as the main converter current supplies the increased VAR, the auxiliary current reduces. It is found from Figs. 5.13 and 5.14 that at increased load the dc link voltage settles to a higher value of 1660 V and comes back to its previous value of 1370 V when the load current is brought back to its earlier magnitude.

The ripple voltage in the dc link is found to be around 3.6%.

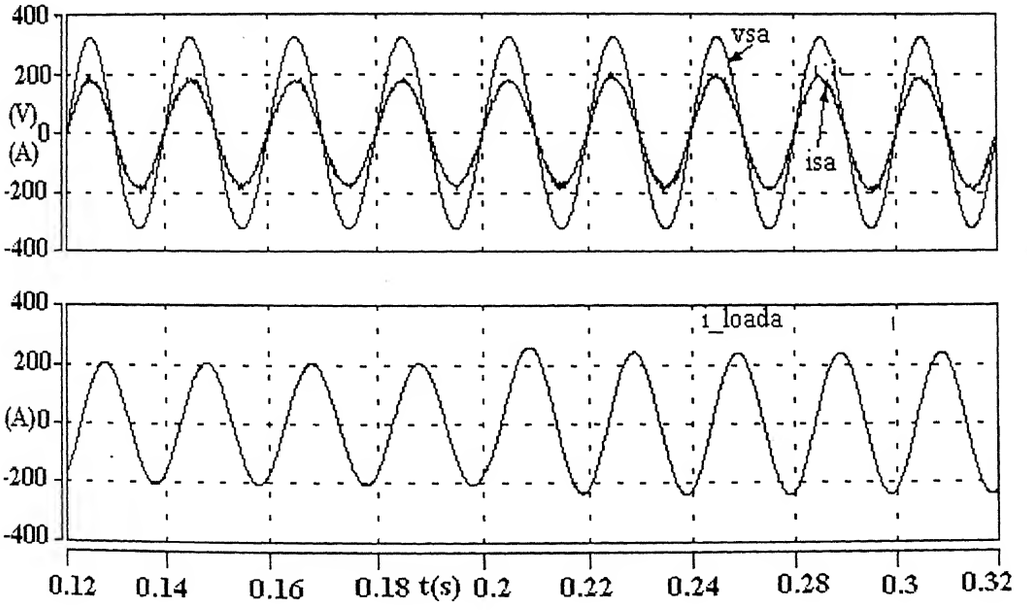

Fig. 5.10 Dynamic response of 6-Step-APF scheme when load current is increased from 145.8 A to 170 A.

vsa = A-phase supply voltage, isa = A-phase supply current

i_loada = A-phase load current

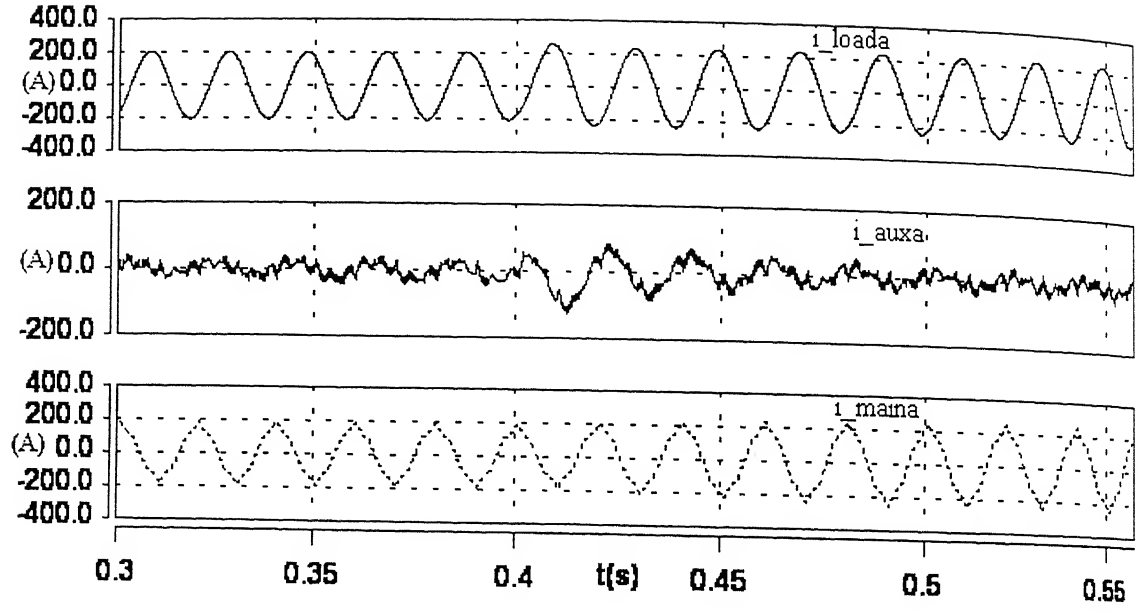

Fig. 5.11 Dynamic response of 6-Step-APF scheme when load current is increased from 145.8 A to 170 A. i_loada = A-phase load current, i_maina = A-phase main converter current, i_auxa = A-phase auxiliary converter current

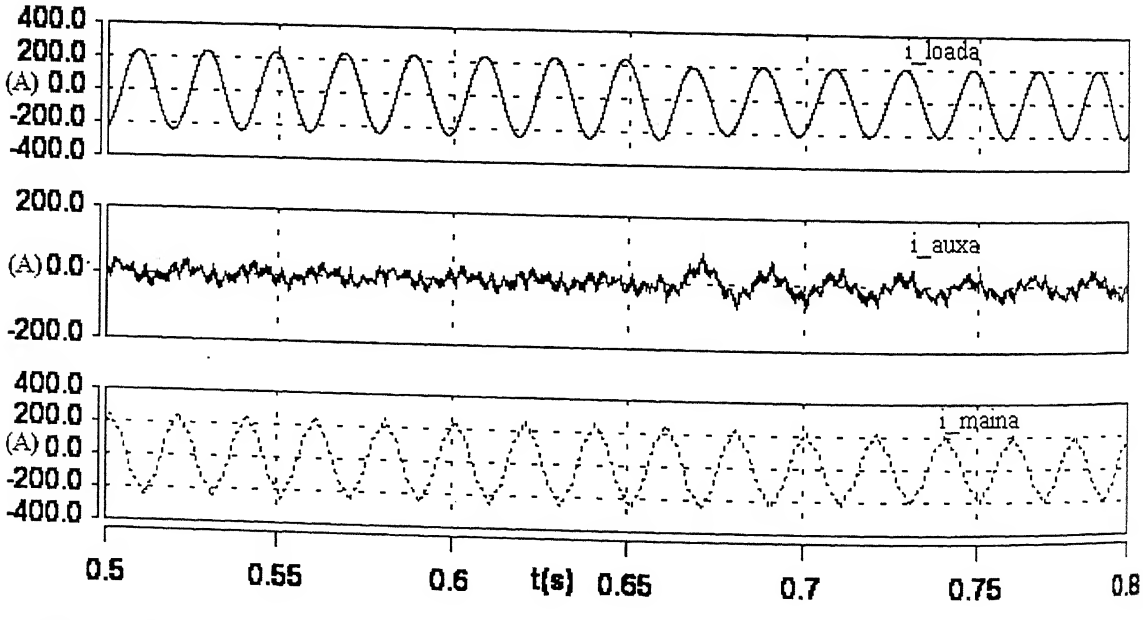

Fig. 5.12 Dynamic response of 6-Step-APF scheme when load current is decreased from 170 A to 145.8 A .

i_loada = A-phase load current, i_maina = A-phase main converter current

i_auxa = A-phase auxiliary converter current

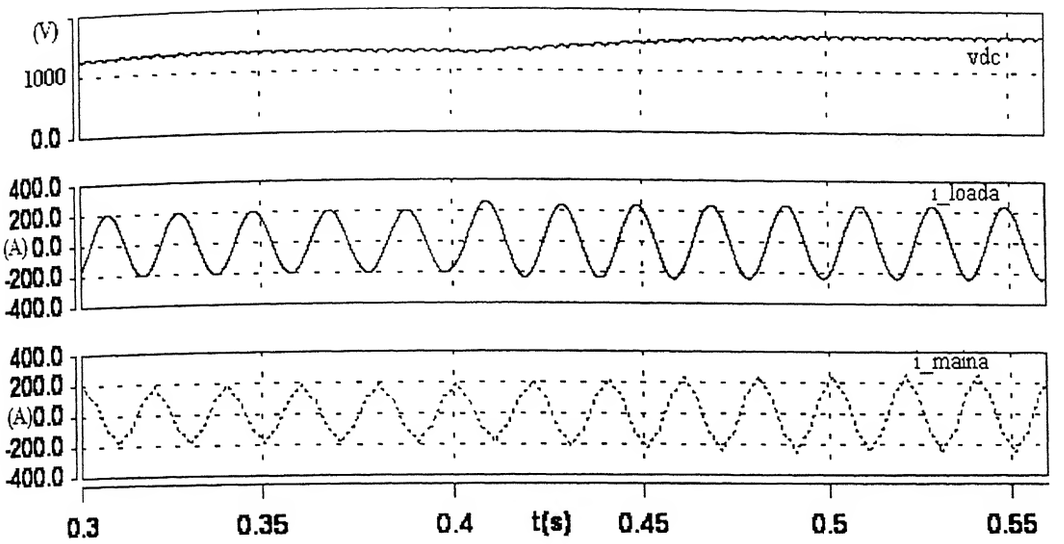

Fig. 5.13 Dynamic response of 6-Step-APF scheme when load current is increased from 145.8 A to 170 A. Vdc = DC link voltage

i_loada = A-phase load current, i_maina = A-phase main converter current

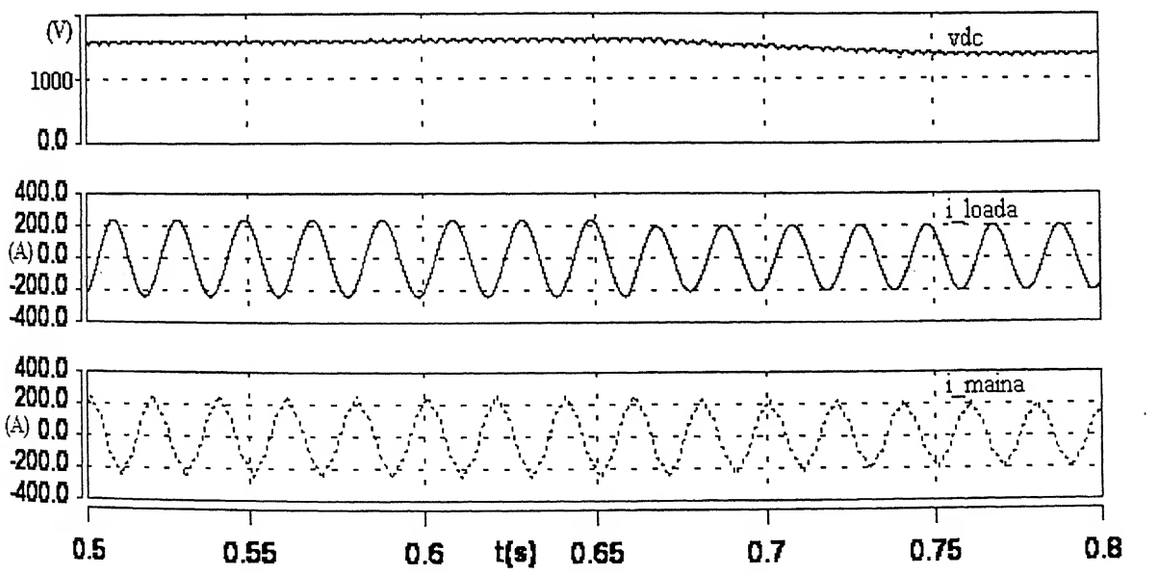

Fig. 5.14 Dynamic response of 6-Step – APF scheme when load current is decreased from 170 A to 145.8 A. Vdc = DC link voltage

i_loada = A-phase load current, i_maina = A-phase main converter current

5.4.2 Performance of NPC-APF for VAR compensation of linear load

Steady State response

Similar load conditions have been tested for NPC-APF converter operation as well. Fig. 5.15 shows the supply voltage and current, which are found to be nearly in phase with each other (0.996 pf). Fig. 5.16 shows that with only NPC converter working, the utility current THD is only 2.8%, which is well within the permissible limit of IEEE-519 standard specification. It is concluded that for VAR compensation for linear load only, a single NPC converter is sufficient.

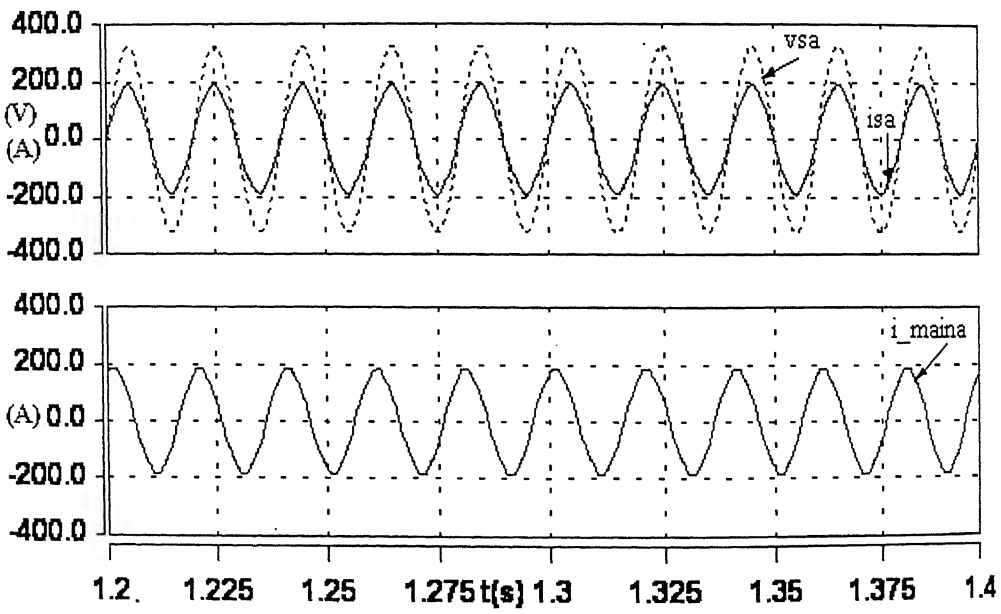

Fig. 5.15 Steady state voltage and current waveform of phase-A in NPC – APF

vsa = A-phase supply voltage, isa = phase-A supply current

i_maina = A-phase NPC converter current

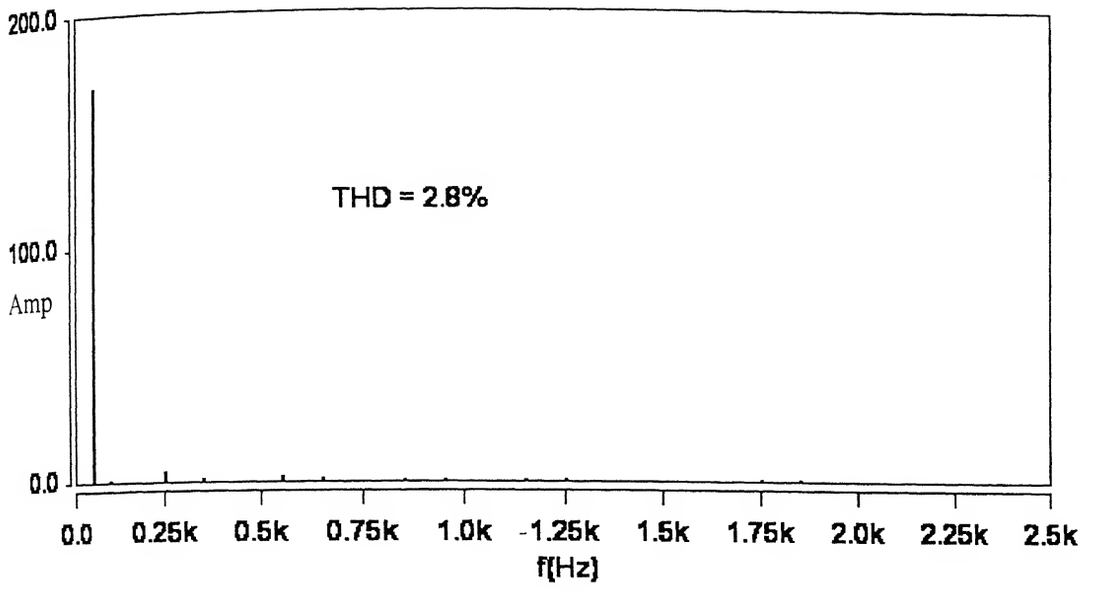

Fig. 5.16 Harmonic spectra of the supply current of phase-A for NPC – APF scheme when auxiliary converter is not connected.

Dynamic Response

Similar change in load current was performed as mentioned in Section 5.4.1 to observe the dynamic performance of the NPC converter. Figs. 5.17 and 5.18 show the NPC converter performance under dynamic load change. As soon as the load current changes, though the converter current starts changing according to requirement, the power factor deviates from unity for 2 cycles as the NPC converter is not directly current controlled. When the load current is increased, the source current becomes little lagging (0.89 lag in simulation).When the load current is brought back to its previous value, the source current becomes leading (typically 0.98, in simulation). The transient changes in the dc link voltage are shown in Figs. 5.19 and 5.20, where with increase in load current the dc link voltage is also increased from 1300 V to 1670 V, and comes back to its previous value when the load current is restored to the previous value. The ripple in the dc link voltage is 7%. Fig. 5.21 shows the individual capacitor voltages (vcap1 and vcap2) along with the total dc link voltage Vdc in steady state condition.

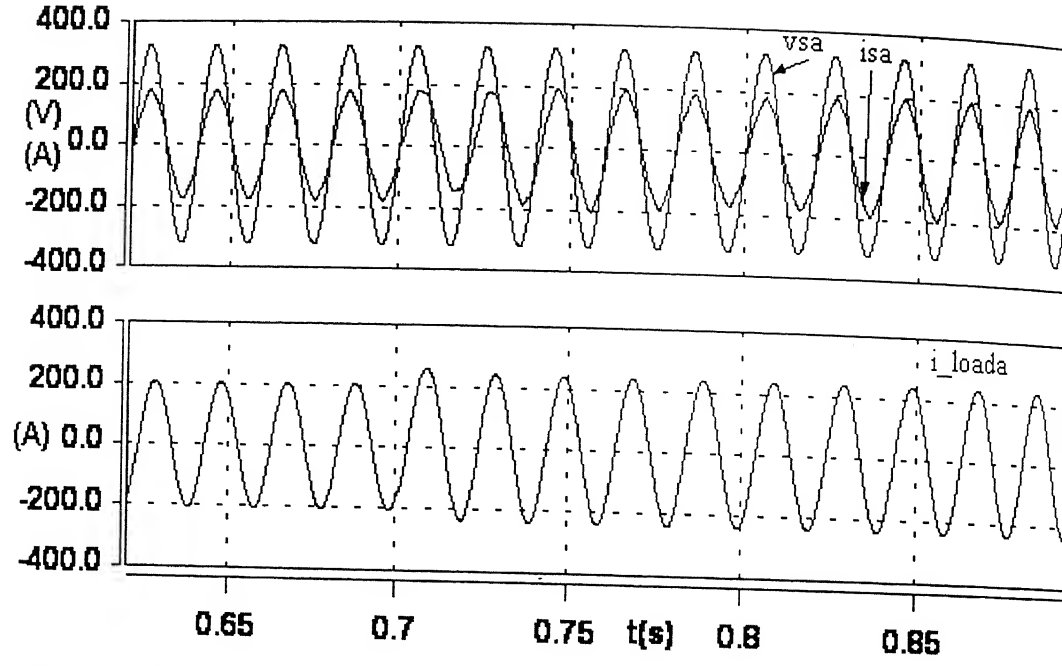

Fig. 5.17 Dynamic response of NPC-APF scheme when load current is increased from 145.8 A to 170 A. vsa = A-phase supply voltage
isa = A-phase supply current, i_loada = A-phase load current

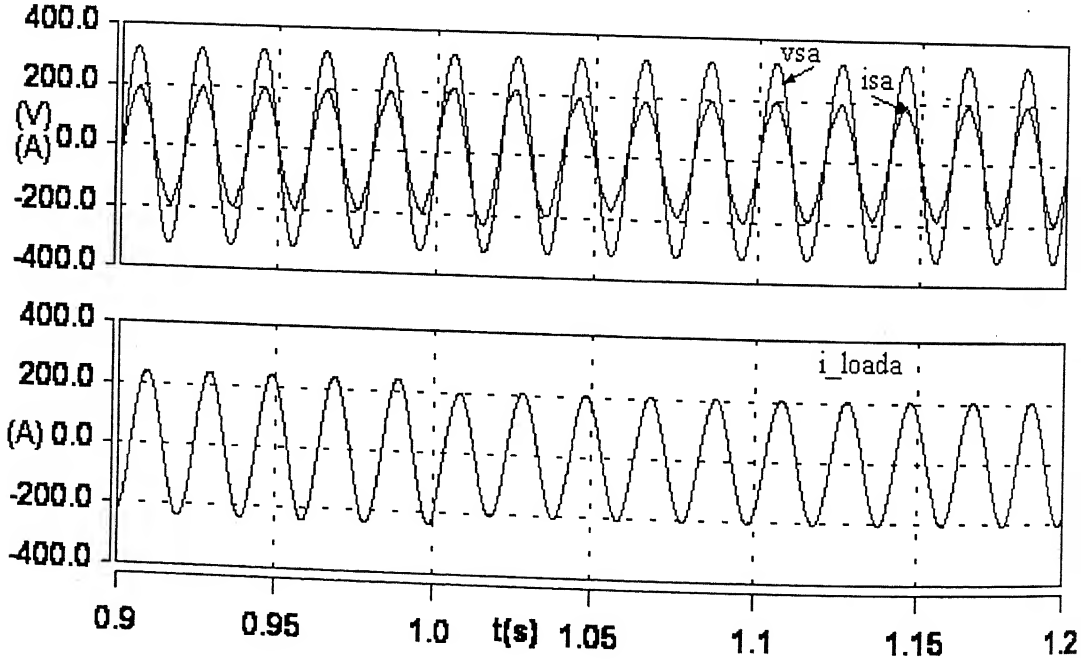

Fig. 5.18 Dynamic response of NPC-APF scheme when load current is decreased from 170 A to 145.8 A. vsa = A-phase supply voltage
isa = A-phase supply current, i_loada = A-phase load current

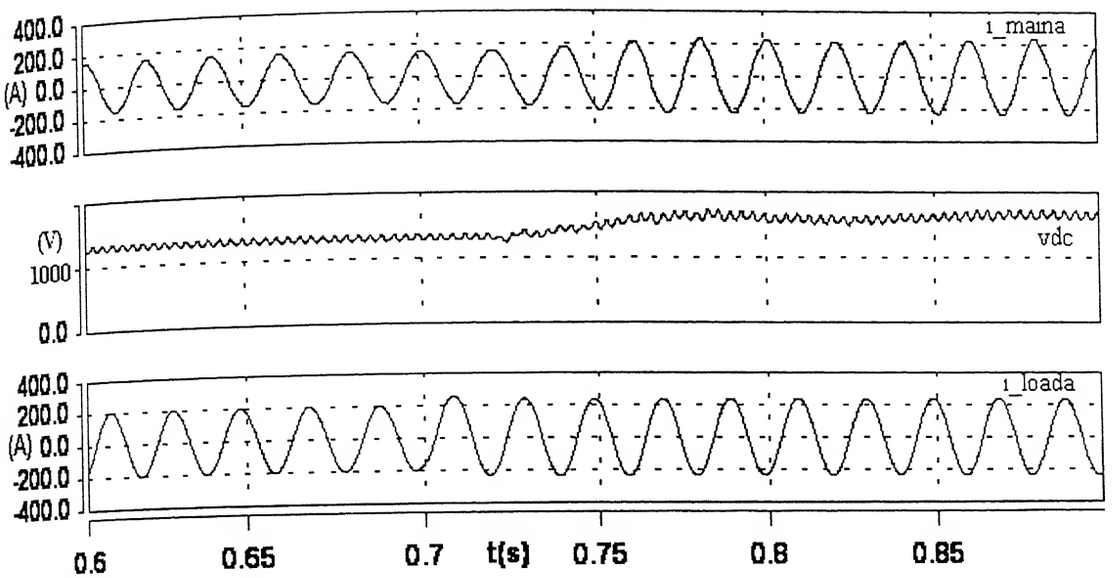

Fig. 5.19 Dynamic response of NPC-APF scheme when load current is increased from 145.8 A to 170 A. Vdc = DC link voltage i_loada = phase-A load current i_maina = phase-A main converter current

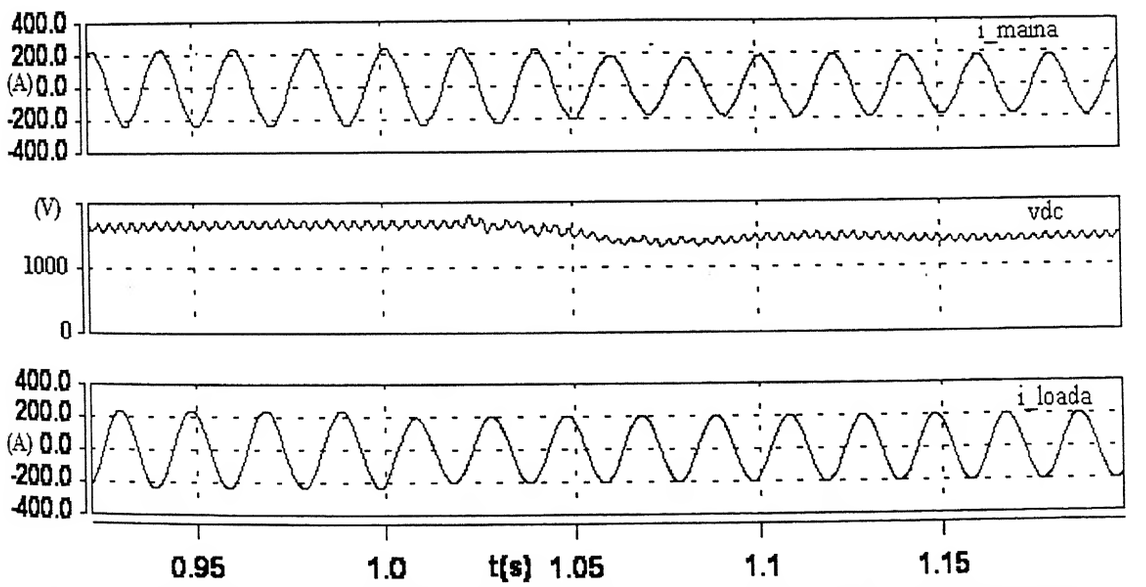

Fig. 5.20 Dynamic response of NPC-APF scheme when load current is decreased from 170 A to 145.8 A. Vdc = DC link voltage i_loada = phase-A load current, i_maina = phase-A main converter current

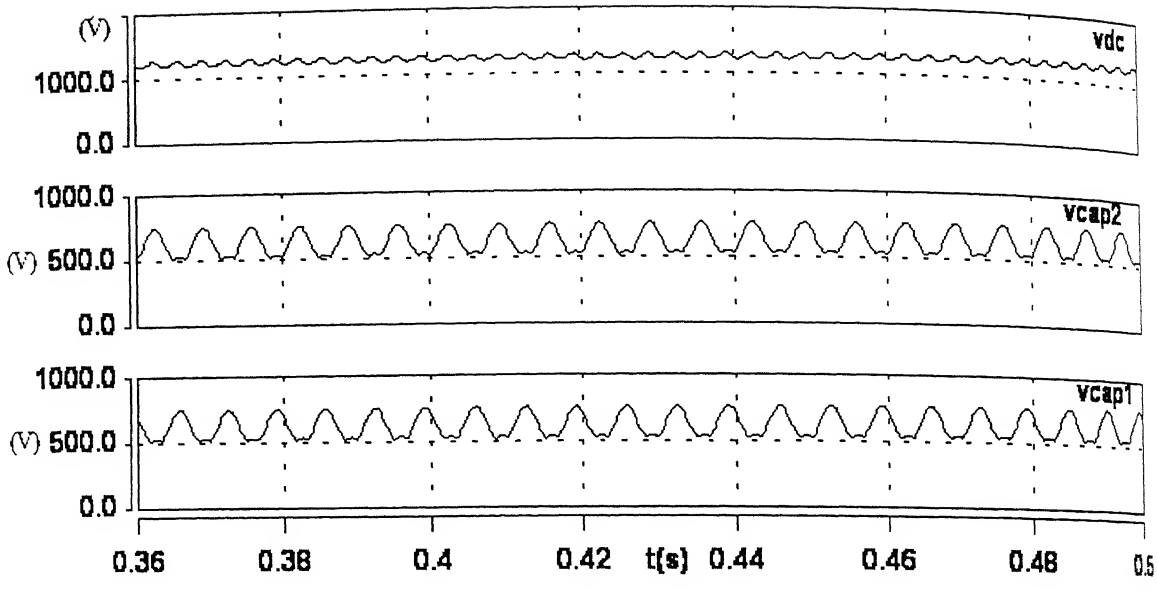

Fig. 5.21 DC link voltage and ripple in capacitor voltages

Vdc = DC link voltage, vcap1 = voltage across capacitor 1

vcap2 = voltage across capacitor 2

Performance comparison of the two schemes (6-Step-APF and NPC-APF) for linear load

It is observed that for the same linear lagging power factor load, NPC converter itself is sufficient to compensate VAR and maintain the desirable current quality of the utility. On the other hand, the six step converter configuration requires the auxiliary converter to take action to reduce the utility current THD below 5%. The ripple in the dc link voltage is found to be more in 6-Step-APF converter for the same value of dc link capacitor. Hence, for linear load, NPC converter alone is sufficient for reactive power compensation with permissible harmonic limits set by IEEE-519.

5.4.3 Performance of 6-Step – APF compensation for non-linear load

The effect of individual converters on utility current and their steady state performance is investigated in this section. A phase controlled rectifier, which consumes 100 kVA, is used as a non-linear load having both large VAR and harmonics in the input current. It is seen that the load current THD is 15.1%. When only the main converter is on, the supply current THD is found to be 18.6% (Fig. 5.22), and after the auxiliary converter is switched on, the supply current THD reduces to as low as 4.6% (Fig. 5.23). The average ratio of auxiliary to main converter current is on an average found to be nearly 25.7%. Fig. 5.24 shows the steady state waveform of source voltage, source current and load current after auxiliary converter is turned on.

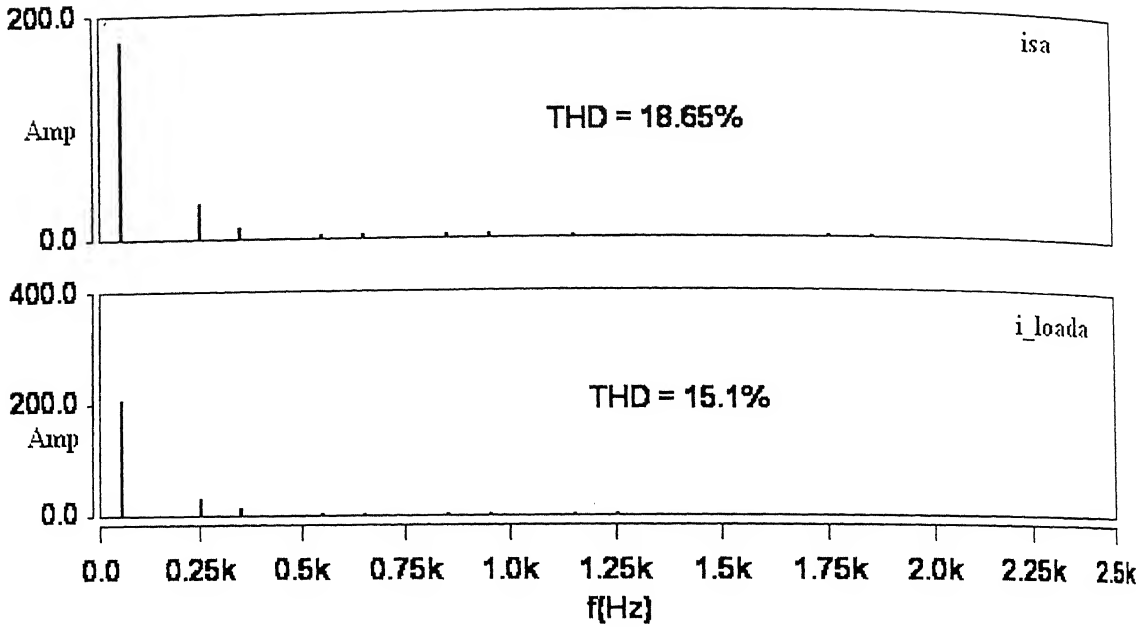

Fig. 5.22 Harmonic spectra of 6-Step – APF scheme for nonlinear load compensation
a) supply current of phase-A (without auxiliary converter), b) load current of phase-A

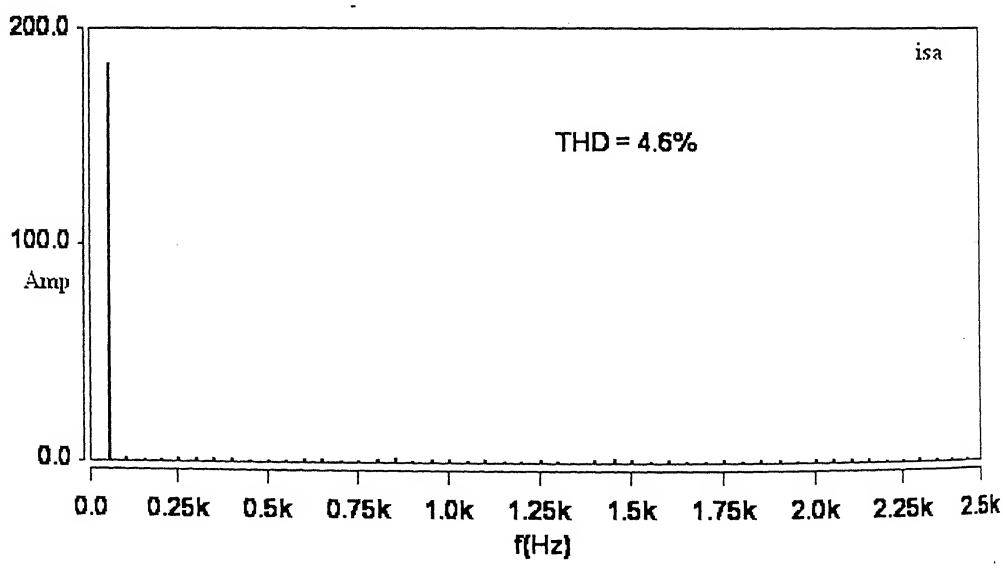

Fig. 5.23 Harmonic spectra of supply current (phase-A) with auxiliary converter ON

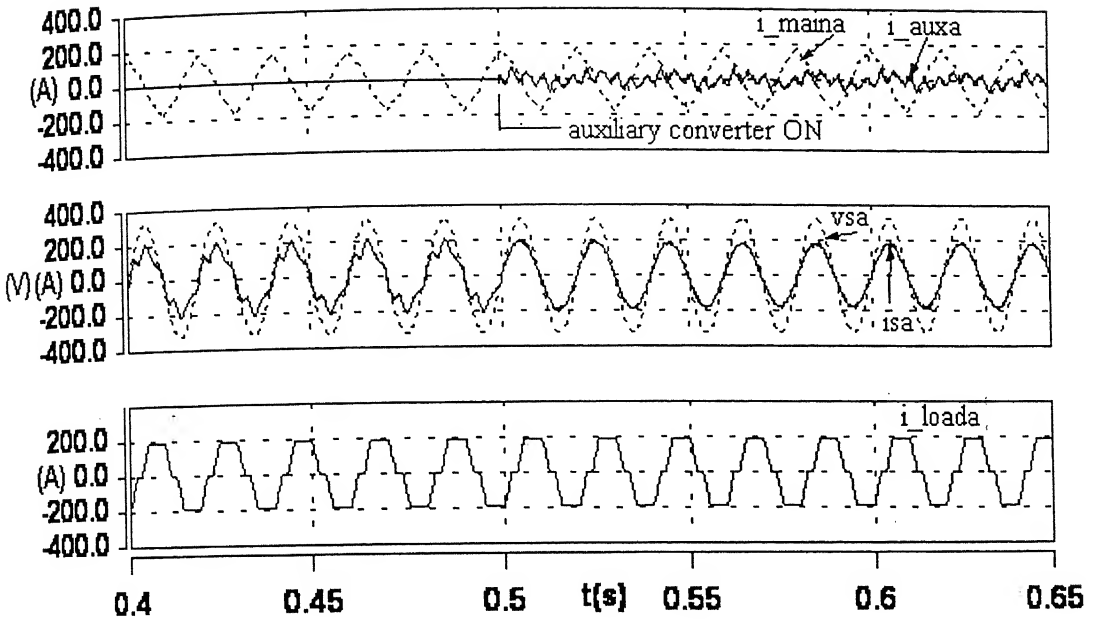

Fig. 5.24 Steady state phase-A supply voltage, supply current and load current waveforms. vsa = phase-A supply voltage
isa = phase-A supply current, i_loada = phase-A load current

Dynamic Performance

The load kVA has been increased from 100 to 120 kVA. Once the two converters lock the utility voltage and current to unity power factor condition, the dynamic change in load is also mitigated at the same condition without change in power factor. Momentarily the transient reactive current demand of the load is taken care by the fast acting auxiliary converter as seen in Figs. 5.25 and 5.26. But as soon as the main converter supplies the increased VAR, the current of the auxiliary converter reduces. Corresponding increase in dc link voltage is observed in Figs. 5.27 and 5.28. Here the dc link voltage changes from 1280 V to 1475 V with the specified change in load current.

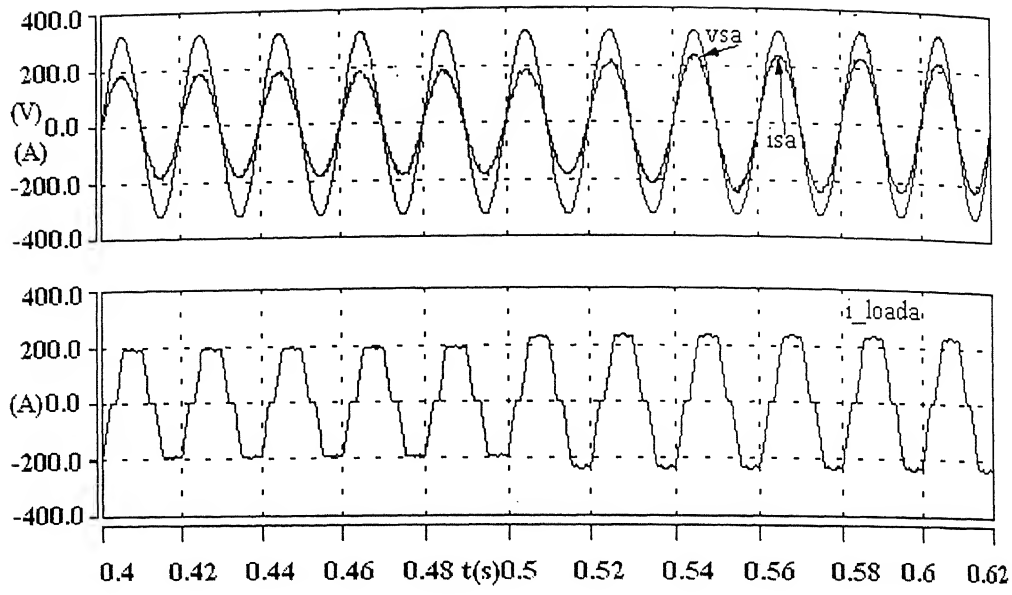

Fig.5.25 Dynamic response of 6-Step-APF scheme when load current is increased from 145.8 A to 170 A. vsa = A-phase supply voltage
isa = A-phase supply current, i_loada = A-phase load current

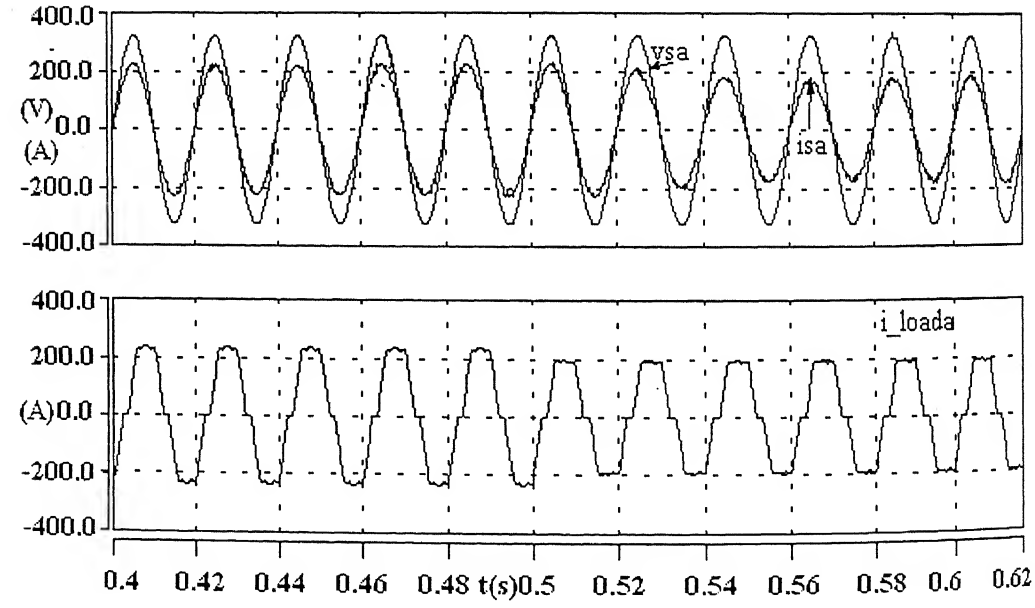

Fig. 5.26 Dynamic response of 6-Step-APF scheme when load current is decreased from 170 A to 145.8 A. i_loada = A-phase load current
i_maina = A-phase main converter current, i_auxa = A-phase auxiliary converter current

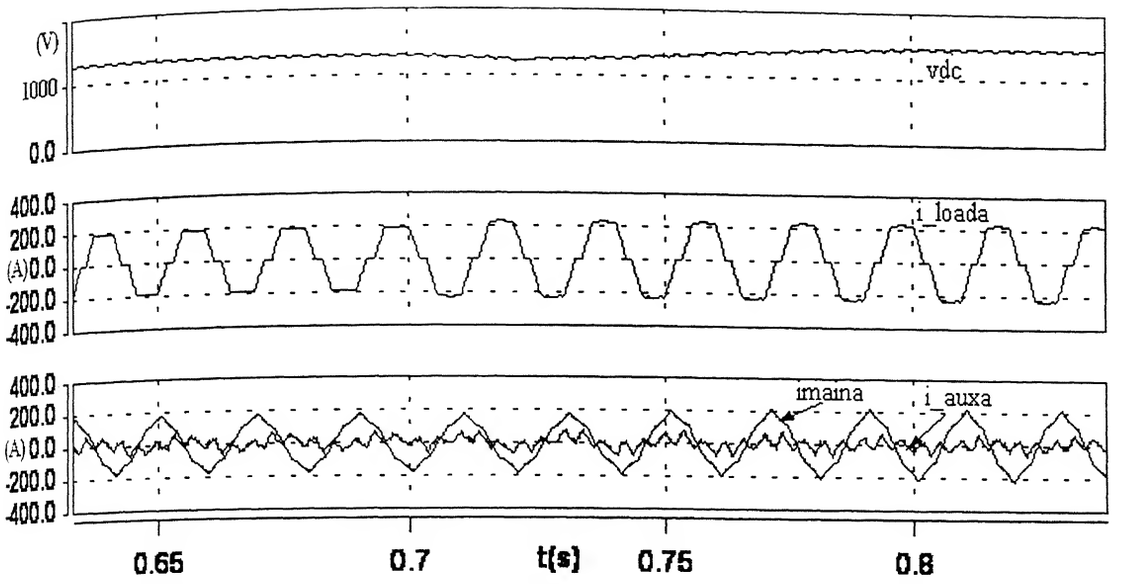

Fig. 5.27 Dynamic response of 6Step – APF scheme when load current is increased from 145.8 A to 170 A, Vdc = DC link voltage, i_loada = A-phase load current i_maina = A-phase main converter current, I_auxa = A-phase auxiliary converter current

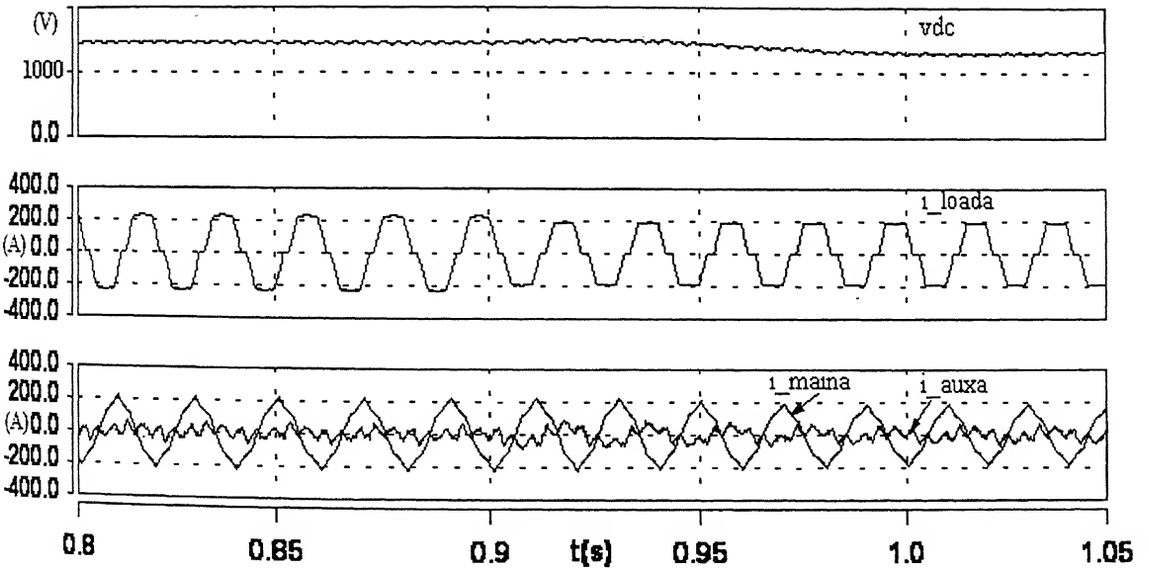

Fig. 5.28 Dynamic response of 6-Step – APF scheme when load current is decreased from 170 A to 145.8 A. Vdc = DC link voltage
i_loada = A-phase load current, i_maina = A-phase main converter current

5.4.4 Performance of NPC – APF scheme compensation for non-linear load

Steady state performance

Fig. 5.29 shows the supply voltage, supply current and load current of phase A. The load current is having displacement factor of 0.66 (lag). The load current rms is 148 A. The total load is close to 100 kVA and the load current THD is 15.1 % (with 5^{th} and the 7^{th} as dominant harmonics as seen in Fig. 5.30). Initially the auxiliary converter is not switched on. The main converter supplies the fundamental reactive current to the load. But the main converter cannot compensate for the current harmonics, and the supply current THD is found to be 17.19% (dominant harmonics are found to be 5^{th} (15.7%), 7^{th} (7.6%)). As the auxiliary converter is switched on, the supply current is confined within a hysteresis band, and then the utility current THD reduces to 4.4% (Fig. 5.31), and supply power factor becomes nearly unity (0.996 p.f.) [74].

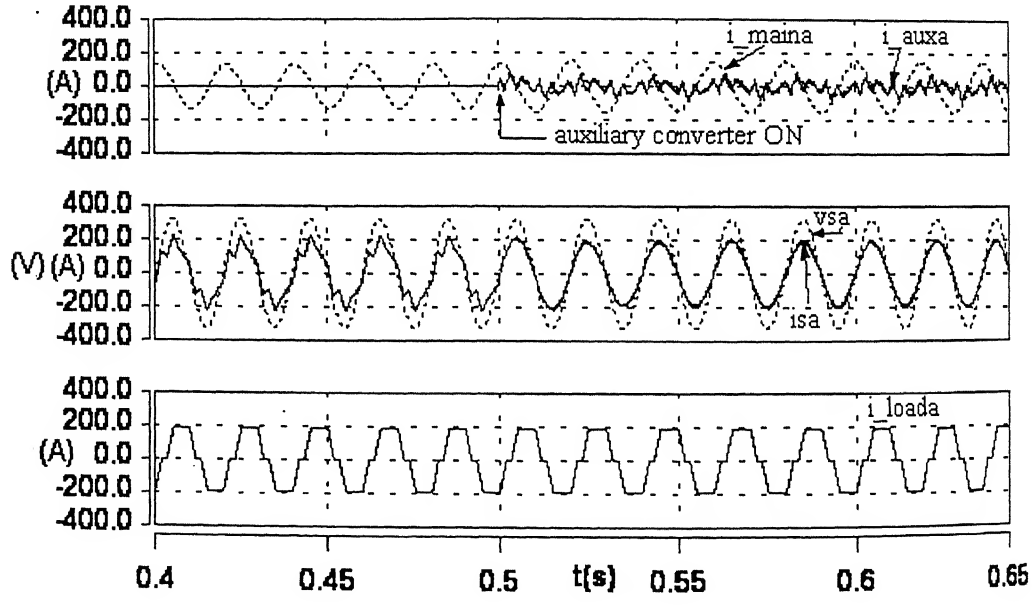

Fig. 5.29 Steady state voltage and current waveform of phase-A in NPC – APF

vsa = A-phase supply voltage isa = A-phase supply current

i_loada = A-phase load current, i_maina = A-phase NPC converter current

i_auxa = A-phase auxiliary current

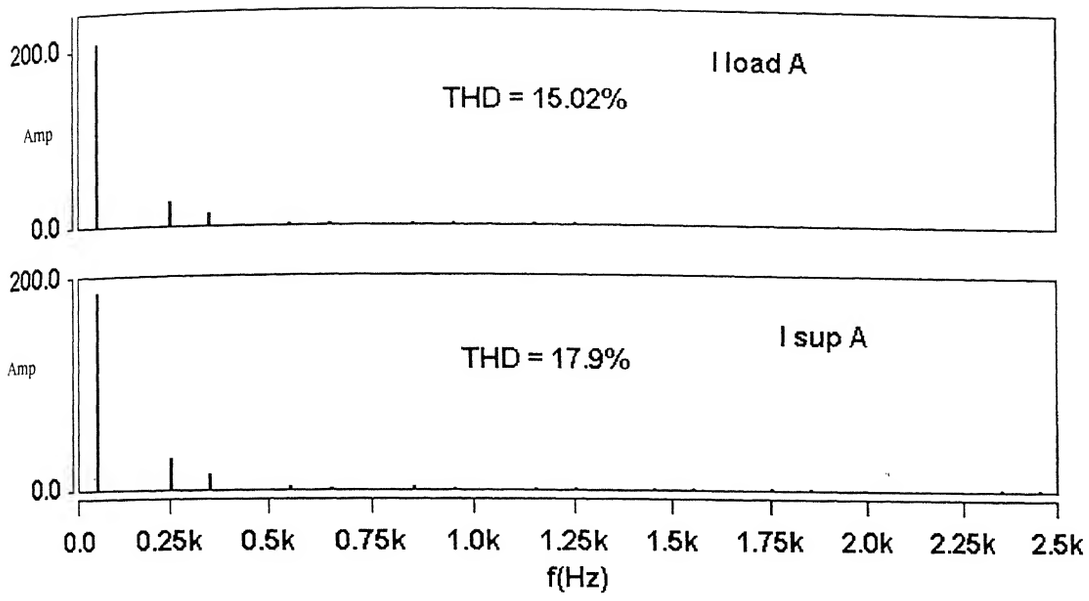

Fig. 5.30 Harmonic spectra of 6-Step – APF scheme for nonlinear load compensation
a) supply current of Phase-A (without auxiliary converter), b) Load current of phase-A

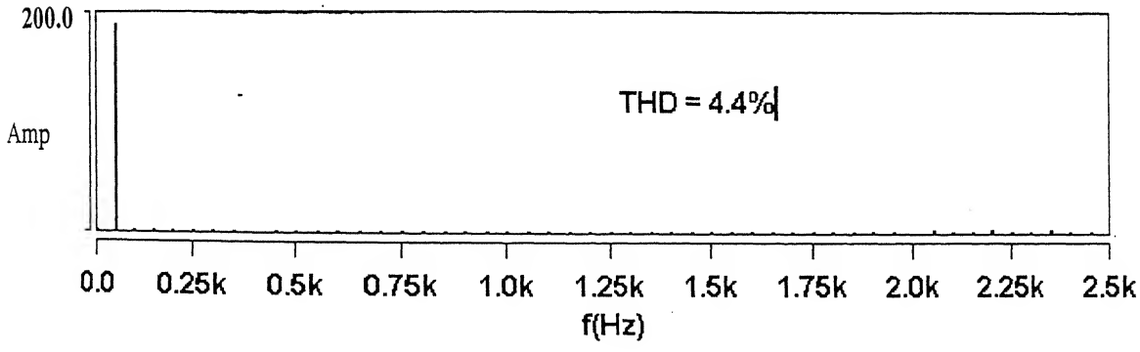

Fig. 5.31 Harmonic spectra of supply current (phase-A) with auxiliary converter ON

At 100 kVA load, the ratio of auxiliary current to the main converter current is around 27%. The dc link voltage is near 1300 V, with peak to peak ripple around 9.3% (Fig. 5.32). It has been observed that the ripple content appreciably reduces to 1.3%, if each capacitor is of 4000 μF.

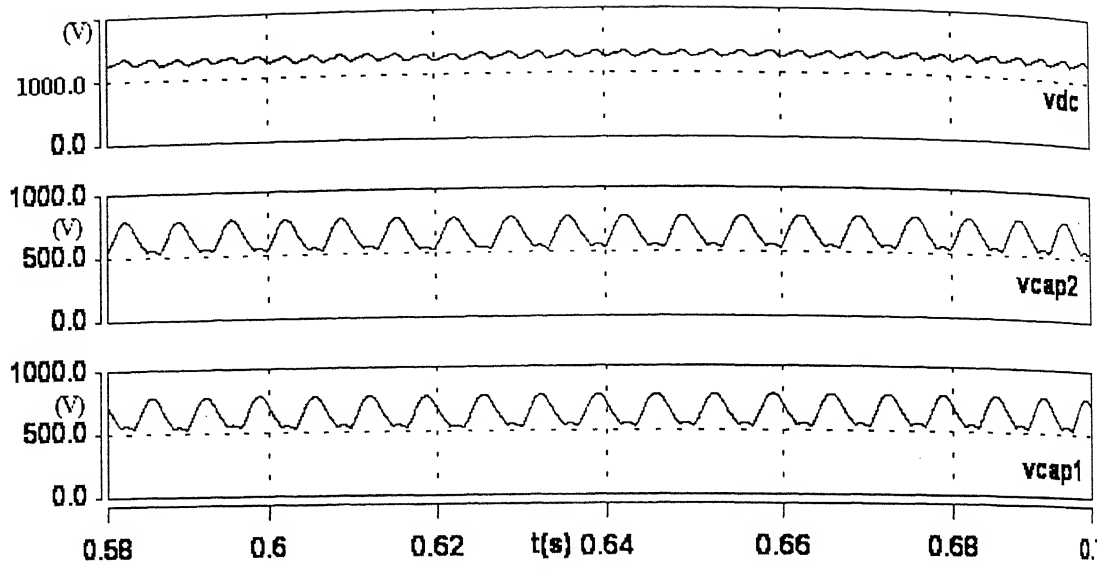

Fig. 5.32 DC link voltage and ripple in capacitor voltages

Vdc = DC link voltage, vcap1 = voltage across capacitor 1

vcap2 = voltage across capacitor 2

Dynamic Performance

The load kVA has been increased from 100 to 120 kVA. Once the two converters lock the utility voltage and current to unity power factor condition, the dynamic change in load is also mitigated at the same condition without change in power factor (Figs. 5.33, 5.34). The transient reactive current demand of the load is taken care by the fast acting auxiliary converter. But as soon as the main converter current supplies the increased VAR, the current of the auxiliary converter reduces. Corresponding increase in dc link voltage is found to be 1300 V to 1500 V.

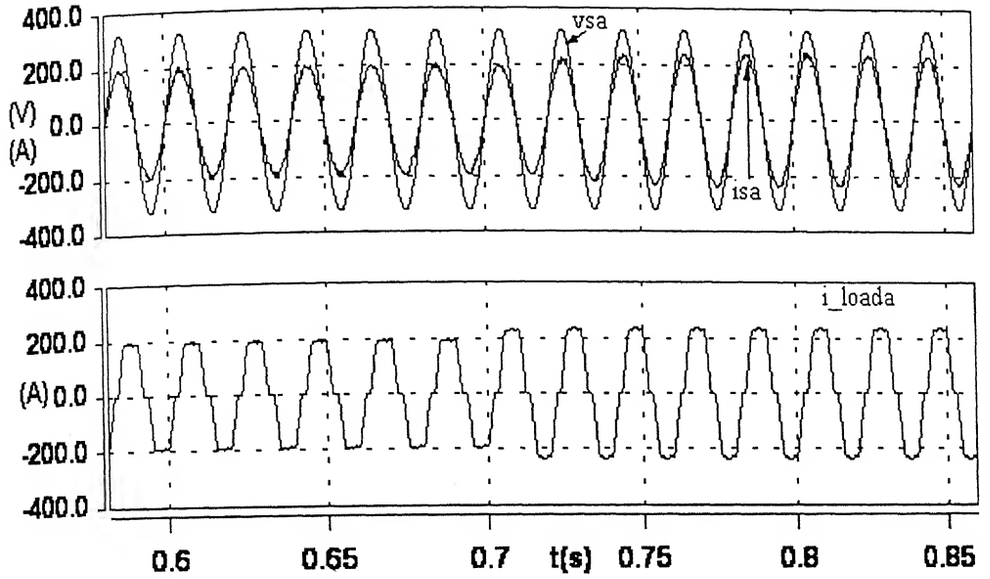

Fig.5.33 Dynamic response of NPC – APF scheme when load current is increased from 145.8A to 170A. vsa = A-phase supply voltage

isa = A-phase supply current, i_loada = A-phase load current

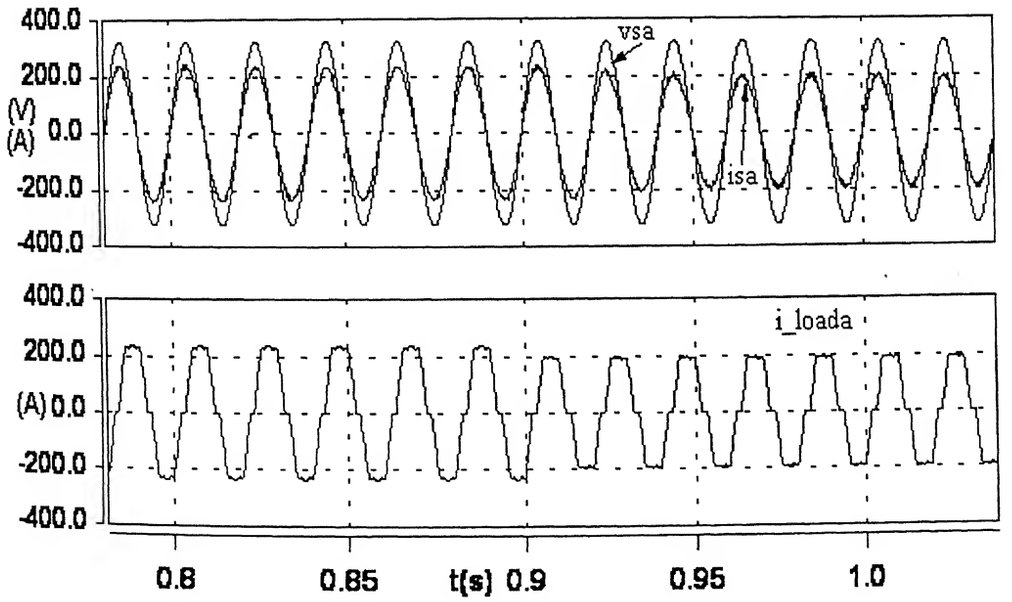

Fig. 5.34 Dynamic response of NPC-APF scheme when load current is decreased from 170 A to 145.8 A, i_loada = A-phase load current

i_maina = A-phase main converter current i_auxa = A-phase auxiliary converter current

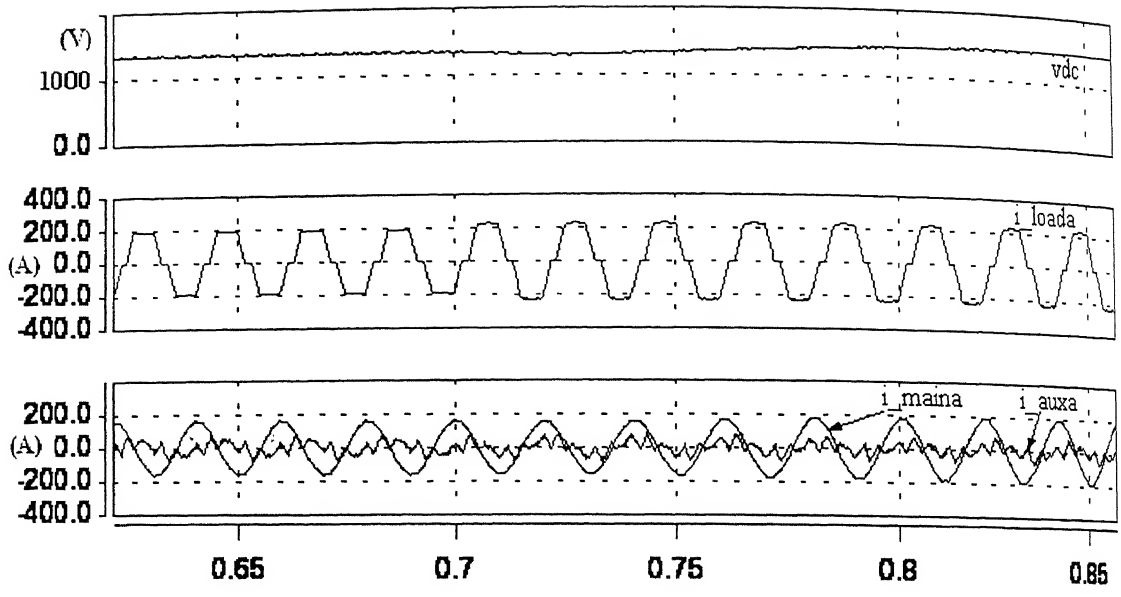

Fig. 5.35 Dynamic response of NPC – APF scheme when load current is increased from 145.8 A to 170 A. Vdc = DC link voltage
i_loada = A-phase load current, i_maina = A-phase main converter current

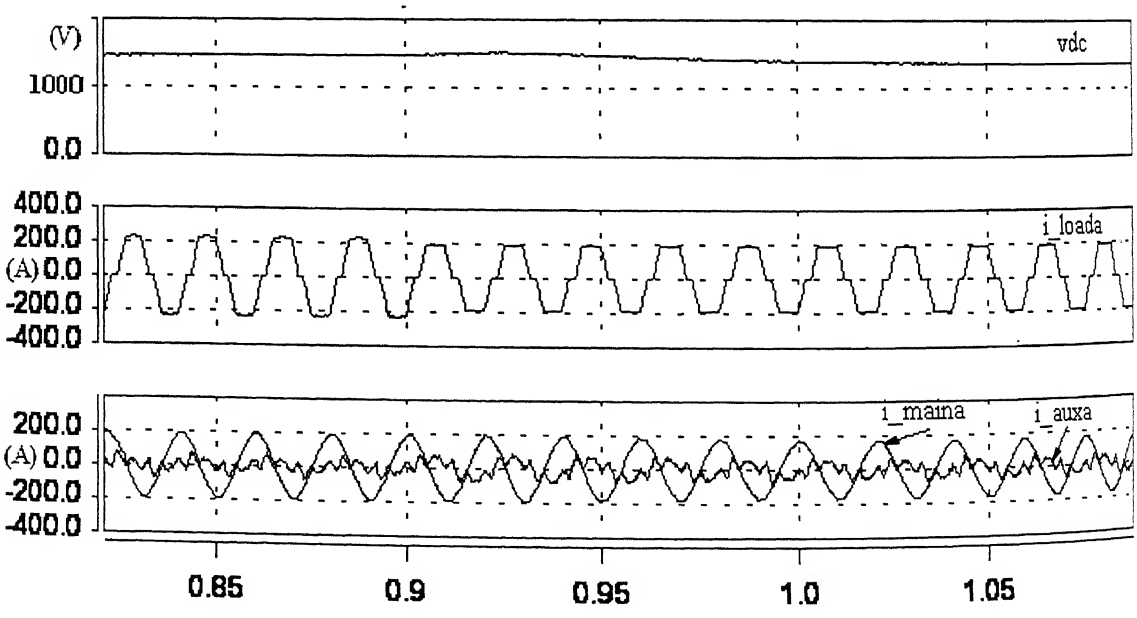

Fig. 5.36 Dynamic response of NPC – APF scheme when load current is decreased from 170A to 145.8A. Vdc = DC link voltage, i_loada = A-phase load current
i_maina = A-phase main converter current, i_auxa = A-phase auxiliary converter current

Performance comparison of the two schemes (6-Step-APF and NPC-APF) for non-linear loads

It is found from the comparative analyses that for nonlinear load, the two topologies are comparable (Table 5.1). The dc link ripple is higher in case of multi level topology, if same value of capacitor is chosen.

5.5 Conclusion

A new parallel converter topology and control strategy has been investigated and reported in the present chapter. This combination of parallel compensator has been shown to be useful for high power loads with large VAR and harmonics, as the combination of high power low frequency devices and low power high frequency devices are utilized to their full capacity.
For linear loads it has been observed that NPC 3 level converter combination provides VAR support to the load and its harmonic content in supply current is below 5%. So, there is no further need to turn on the auxiliary converter. But during transient load change conditions, the input power factor would deviate from unity, as the NPC converter is not directly current controlled. As the dynamic response is fast, within 2-3 cycles, the input power factor is restored to unity.

The performances of the two converter combinations are comparable for non-linear loads, having large harmonics. Thus, the combination of APF scheme proposed in this chapter is found to be very effective for high power load compensation. A summary table (Table 5.1) has been given with comparative performance of the two schemes.
The combination of APF scheme proposed in this chapter is found to be useful for high power load compensation.

Table 5.1

Performance comparison of 6-Step-APF and NPC-APF on 400V system

Rating andType of load	Load current THD	Supply current THD With only 6-Step	Supply current THD With 6-Step & Auxiliary	Ratio of Auxiliary current to Main current	Supply current THD With only NPC	Supply current THD With NPC & Auxiliary	Ratio of Auxiliary current to Main current
Linear Load 100 kVA 0.634 p.f. lag	-	7.2%	4.59%	14% (18.8/129.69)A	2.8%	Not Required to operate	-
Non-linear Load 100 kVA phase angle 30° lag	15.1%	18.65%	4.6%	25.7%	17.9%	4.4%	27%

Chapter 6

Conclusion

6.1 General Conclusions

Power Quality Control (PQC) has emerged as a major area of global research concern due to the trend of increasing use of non-linear and harmonic producing loads over last two decades. These loads distort the voltage waveform at the point of common coupling (PCC), increase line losses and losses in transformers, leading to reduced efficiency and reliability. The advancement of sophisticated, automated process control has made industrial loads more voltage sensitive and susceptible to supply voltage variations. International agency specified standards are being developed for favorable PCC voltage and current. Also, PQ surveys are performed to identify the problem areas, which require protective and remedial measures. The findings have given impetus to develop custom power equipment for better utility interface.

Active Power Filters (APF) have been widely investigated for load current harmonic elimination and power factor correction. Dynamic Voltage Restorers (DVR) have been applied to protect the voltage at the PCC from supply voltage variation (in particular voltage sag). The third category of equipment is a unified scheme, which keeps the utility current clean by load harmonic isolation and makes the load end voltage insensitive to supply voltage variation. Though conceptually these types of Unified Power Quality Conditioners (UPQC) are combinations of APFs and DVRs, the implementation aspects require extensive investigations for successful performance and coordinated control realization of the equipment. This area, being relatively unexplored, has been taken up as the scope of investigation of the present dissertation.

6.2 Contributions of the Present Work

The present dissertation has reported the development of single phase and three phase topologies of Unified Power Quality Conditioners with a self sustaining dc bus. The thesis

has presented in detail the design, simulation and a prototype laboratory implementation of UPQC.

The features of the developed UPQC are summarized as follows.

- Results have been presented to show that UPQC eliminates the harmonics in the supply current, provides local VAR support, and thus improves utility current quality for nonlinear loads. The analog hysteresis current control scheme of the shunt compensator has been successful in keeping the utility current THD below the specified standard and utility power factor very close to unity.

- The load voltage has been maintained to the desired level by injecting a suitable voltage through the series compensator of the UPQC in presence of balanced supply voltage sag. The **first** proposed **scheme** of UPQC **(UPQC-Q)** injects the voltage in quadrature advance to the supply current so that the series compensator does not consume any real power in the steady state. Additionally, the series compensator shares VAR of the load with the shunt compensator, and thus, the VA loading on the shunt compensator is somewhat reduced.

- The self supporting dc link capacitor voltage (charge maintained by the shunt compensator) is a big advantage for UPQC-Q in under-voltage conditions. Hence, the duration of under-voltage or sag is not a constraint of operation. This is different from most of the schemes reported in the literature on DVRs, where the dc link voltage is supported from external battery source.

- The present dissertation has reported a control scheme suitable for both single phase as well as three phase applications. A PC–based closed-loop hybrid controller has been proposed, combining analog and digital controllers, having good accuracy, speed, flexibility and ease of implementation. A dynamic sag controller has been designed, through a closed-loop PI controller that ensures the phase quadrature relationship in case of variable voltage sag and variable load. Extensive SABER simulation results have been presented and typical simulation results are validated by experimental results.

The **second UPQC control scheme (UPQC-P)** with in-phase voltage injection for *unbalanced sag mitigation* has been designed and simulated in SABER. d-q-o component based synchronously rotating frame analysis has been adopted in this case for dynamic sag controller, with a closed loop control to ensure appropriate voltage injection. During a balanced voltage sag, the injected voltage is found to be in phase with the supply current, therefore the series compensator acts as an active power consuming device only and becomes a dc load to the dc link capacitor. A detailed VA loading analysis has been carried out for different load power factor and sag conditions. Results confirm the effectiveness of the proposed control technique.

The last part of the dissertation has reported an efficient utilization of parallel converters as VAR compensators and Active Power Filters (APF) for large power loads. A novel parallel converter topology with a three-level Neutral Point Clamped (NPC) converter and an auxiliary current controlled VSI has been proposed and control techniques have been developed. Extensive simulation study has been carried out in SABER simulator for linear and non-linear loads, and performance has been compared with a combination of standard six-step main converter and the auxiliary converter. The results show the effectiveness of the control scheme for achieving low THD of the utility current as specified by IEEE standard. This study is useful in the design of UPQC for high power applications.

6.3 Scope for Further Work

The investigation of the present dissertation can be continued in the following areas.

1. Implementation of UPQC-P scheme with a suitable DSP controller can be a potential area of research.
2. Design and implementation of UPQC for variable phase angle voltage injection facility such that both sag and swell can be taken care of.
3. Experimental investigation of the parallel converter schemes (as reported in Chapter 5) for high power application.

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Appendix-A

Voltage and Current Sensor Specifications

A-1 Voltage Sensor

PCB Mounting Hall Effect Voltage Transducer (Model LV 25-P)

Technical Specifications:

Nominal current I_N	:	10 mA
Nominal analogue output current	:	25 mA
Turns ratio	:	2500:1000
Overall accuracy at 25°C	:	± 0.6% of I_N
Supply Voltage	:	± 15 V (± 5%)
Isolation	:	2.5 kV (rms)/50 Hz/1 min
Linearity	:	< 0.2%
Response time	:	< 40μ s for R1 series 25 kΩ resistor
Operating temperature	:	0°C to 70°C
Current Consumption	:	10 mA + output current
Primary internal resistance	:	250Ω (at 70°C)
Secondary internal resistance	:	110Ω (at 70°C)
Weight	:	22g
Operating range	:	10 to 500 V

Polarity marking : A positive output current is obtained on terminal M when a positive voltage is applied on terminal +HT of the primary circuit.

Primary resistor R_1 : The transducer's optimum accuracy is obtained with the nominal primary current. As for as possible, R1 should be calculated so that

the nominal voltage to be measured corresponds to a primary current of 10mA.

Measuring resistance		R_M min.	R_M max.
with ± 15 V	at ± 10 mA max.	100Ω	350Ω
	at ± 14 mA max.	100Ω	190Ω

Connection pins

Pin + : Supply voltage +15 V

Pin M : Measuring point

Pin - : Supply voltage -15 V

Pin + HT : Primary voltage +

Pin - HT : Primary voltage -

A-2 Current Sensor

LEM Module LA 55-P

This current transducer can be used for electronic measurement of currents: DC, AC, IMPL., etc., with galvanic isolation between the primary (high power) and the secondary (electronic) circuits.

Electrical Data

Nominal current IN : 50A

Measuring Range : 0 to ± 70 A at 70°C

Measuring resistance		: at + 70°C		at + 85°C	
		R_M min.	R_M max.	R_M min	R_M max.
With ± 12 V	at ± 50 A max.	10Ω	100Ω	60Ω	95Ω
	at ± 70 A max.	10Ω	50Ω	60Ω	60Ω
With ± 15 V	at ± 50 A max.	50Ω	160Ω	135Ω	155Ω
	at ± 70 A max.	50Ω	90Ω	135Ω	135Ω

Nominal analog output current : 50 mA

Turns ratio : 1:1000

Accuracy at +25°C and at ± 15 V (± 5 %) : ±0.65 % of I_N

Turns ratio	:	1:1000
Accuracy at +25°C and at ± 15 V (± 5 %)	:	±0.65 % of I_N
Accuracy at +25°C and at ± 12 V to ± 15 V	:	±0.9 % of I_N
Supply voltage	:	+ and - 12 to 15 V (± 5 %)
Isolation between primary and secondary	:	2 kV rms/50 Hz/1 min.

Accuracy-Dynamic performance

Zero offset current at ± 25°C	: max. ± 0.2 mA	
Residual current after an overload of 3x I_N	: max. ± 0.3 mA	
Thermal drift of offset current		
(between 0°C and +70°C)	: typical ± 0.1 mA	max. ± 0.5
mA		
(between -25°C and +85°C)	: typical ± 0.1 mA	max. ± 0.6
mA		
Linearity	: better than 0.15%	
Response time	: inferior at 500nS	
Rise time	: better than 1μs	
di/dt accuracy followed	: better than 200 A/μs	
Band width	: 0 to 200 kHz (-1dB)	

General Data

Operating temperature	: -25°C to +85°C
Storage temperature	: -40°C to +90°C
Current consumption	: 10 mA (at ± 15 V) + output current
Secondary internal resistance	: 80Ω (at +70°C), 85Ω (at +85°C)
Weight	: 18g

Appendix-B

Filter Phase Shift Calculation

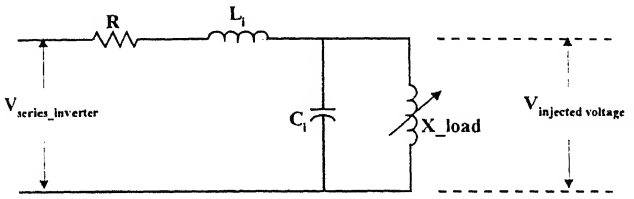

Fig. B-1 Low pass filter configuration

In UPQC-Q, the injected voltage is in quadrature with respect to supply current (voltage). Therefore, the series compensator finds the variation of utility current as a form of variable inductive reactance (X_load) across its filter capacitor (C_i). L_i is the inductance of the low pass filter, which is connected at the output of the series compensator and before the injection transformer. R is the resistance of the transformer which appears in series with the inductor L_i. The leakage inductance of the transformer can also be clubbed with L_i. The magnetizing inductance of the transformer that comes parallel to the filter capacitor will not affect the impedance much as it is very large compared to the other components of the parallel branch (namely C_i and X_load).

The combined impedance of the parallel branch of filter configuration of Fig. B-1 is given by

$$Z_{parallel} = [-jwC_i \| X\_load] \qquad \text{(b-1)}$$

Then the transfer function $F = \frac{V_{injecetd\_voltage}}{V_{series\_inverter}}$ is given by the following equation

$$F = \frac{Z_{parallel}}{R + jwL_1 + Z_{parallel}} \qquad \text{(b-2)}$$

The phase angle of F gives a measure of phase shift according to which the phase of the nominal modulating signal is calculated.

Appendix-C

IGBT Driver Circuit

Fig. C-1 shows the IGBT driver circuit, which converts the low power switching signal from control circuit to the level sufficient to drive the IGBT switch. Also it provides the over-current protection for the IGBT. Opto-coupler 6N137 provides the electrical isolation between the control circuit and the power circuit. Under normal operating conditions, low power drive signals from control circuit are amplified with the help of op-amps U1 and U2 (LM339) and transistors T1 and T2 [75]. Under over-current and fault conditions, diode

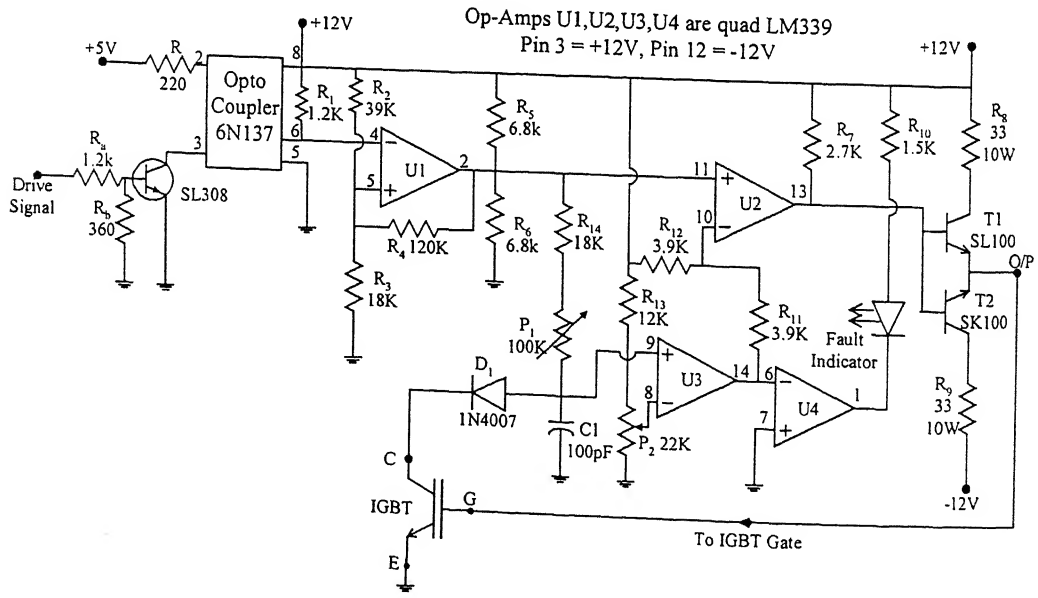

Fig. C-1: IGBT gate driver circuit

D1 is turned off due to large voltage drop across C and E terminals of IGBT and hence the voltage across the capacitor C1 becomes higher than the voltage at pin8 of U3 forcing its output to go high. This results in a higher voltage at the pin 10 of U2 than pin 11, making its output low and thus turning off IGBT. Further the high voltage at pin 6, which is connected to pin 14, makes the output of op-amp U4 low, forcing the fault indicator to glow.

Appendix-D

PCL-208 High Performance Data Acquisition Card

PCL-208 is a high performance, high speed, and multifunction data acquisition card for the IBM PC/XT/AT or compatibles.

Specifications:

1 Analog Input (A/D Converter)

Channels	:	16 Single-ended or 8 Differential, switch selectable
Resolution	:	12 bit
Input Range	:	Unipolar: +10 V, +5 V, +2 V, +1 V. Bipolar: +/- 10 V, +/- 5 V, =/- 2.5 V, +/- 1 V, +/- 0.5 V All input ranges are switch selectable.
Over voltage	:	Continuous +/- 30 V Max.
Conversion Type	:	Successive Approximation
Conversion Speed	:	60 kHz max. (PCL-208 Standard) 100 kHz max. (PCL-208)
Accuracy	:	0.01% of reading +/- 1 bit
Linearity	:	+/- 1 bit
Trigger Mode external (low)	:	Software trigger, on board programmable timer or trigger (TTL compatible, load 0.4 mA max. at 0.5 V or 0.05 mA max. at 2.7 V (high).
Data Transfer	:	Program control, Interrupt control or DMA

2 Analog Output (D/A Converter)

Channels	:	2channels

Resolution	:	12 bit
Output Range	:	0 to + 5 V with fixed - 5 V reference. +/- 10 V with external DC or AC reference.
Reference Voltage	:	Internal: - 5 V (+/- 0.05 V). External: DC or AC, +/- 10 V max.
Conversion Type	:	12 bit monolithic multiplying (DAC 7541)
Linearity	:	+/- 1/2 bit.
Output Drive	:	+/- 5 mA max.
Settling Time	:	5 microseconds.

3 Digital Input

Channel	:	16 bit
Level	:	TTL compatible.
Input Voltage	:	Low - 0.8 V max High - 2.0 V min
Input load	:	Low - 0.4 mA max. at 0.5 V High - 0.05 mA max. at 2.7 V

4 Digital Output

Channel	:	16 bit
Level	:	TTL compatible
Output Voltage	:	Low - Sink 8 mA at 0.5 V max. High - Source -0.4 mA at 2.4 V min.

5 Programmable Timer/Counter

Device	:	INTEL 8254
Counters	:	3 channels, 16 bit. 2 channels permanently connected to 1 MHz /10 MHz clock as programmable pacer, 1 channel free for user application
Input Gate	:	TTL/DTL/CMOS compatible
Time Base	:	10 MHz or 1 MHz, switch selectable.
Pacer Output	:	71 minutes/pulse to 2.5 MHz

6 Interrupt Channel

Level	:	IRQ 2 to 7, software selectable.

Enable	:	Via INTE of CONTROL register.

7 DMA Channel

Level	:	1 or 3 switch selectable
Enable	:	Via DMAE of CONTROL register.

8 General

Power Consumption	:	+ 5 V: typ. 700 mA, max. 1 A. + 12 V :typ. 140 mA, max. 200 mA -12 V : typ. 14 mA, max. 20 mA
I/O Connector	:	20 pin flat cable connector for all Analog/Digital I/O ports
I/O Base Address is	:	Requires 16 consecutive address locations. Base address defined by the DIP switches for address lines A9-A4. (Factory setting is &H300)

Appendix-E

PCL-726 Six Channel D/A Output Card

Specifications

1. Analog output

Channels	:	6 channels
Resolution	:	12 bits. Double buffered
Output range	:	0 to +5 V (Unipolar)
		0 to +10 V (Unipolar)
		+/- 5 V (bipolar)
		4 to 20 mA current loop (sink)
		+/-10 V with external DC or AC reference

2. Reference voltage

Internal	:	-5 V (+/- 0.05 V)
		-10 V (+/- 0.05 V)
External	:	DC or AC, +/- 10 V max.
Conversion type	:	12 bit monolithic multiplying
Linearity	:	+/- ½ bit
Accuracy	:	+/- 0.012% full scale range
Temperature drift	:	2 PPM/deg C full scale range
Settling time	:	70 μsec max. with op-07 output amplifiers
Current loop	:	4 to 20 mA constant current sink
Voltage output drive	:	+/- 5 mA max.
Current loop excitation Voltage	:	minimum +8 V, maximum 36 V for 4 to 20 mA current loop
Reset (Power-on status)	:	All D/A channels will be at 0 V output after reset or power–on , either bipolar or unipolar mode.

3. Digital input

Channel	:	16 bits
Level	:	TTL compatible
Input low	:	0.8 V max.
Input high	:	2.0 V min.
Input load	:	-0.4 mA max. at 0.5 V
		0.05 mA max. at 2.7 V

4. Digital output

Channel	:	16bits
Level	:	TTL compatible
Output low	:	0.5 V max. when sink 8 mA
Output high	:	2.4 V min. when source 0.05 mA

5. General Specifications

Power consumption	:	+5 V : 500 mA typ. 1A max.
		+12 V : 50 mA typ. 110 mA max.
		-12 V : 14 mA typ. 90 mA max.
I/O connector	:	20 pin header for Analog/Digital I/O ports
I/O base address	:	Requires 16 consecutive address locations. Base address
		definable by the DIP switches for address line A8-A4.
		(Factory setting is HEX 2C0).

About the Author

Malabika Basu was born in Kolkata on September 25, 1972. She received the B.E. (Electrical Engg.) and M.E. (Electrical Machines) from Bengal Engineering College, West Bengal, India, in 1995 and 1997, respectively.

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